

Power Devices

Bipolar Gate Drives for Discrete GaN HEMTs

High-voltage enhancement-mode GaN HEMTs are frequently used in applications where hard commutation between power devices is present. The combination of a low gate threshold voltage and a high V_{ds} slew rate can raise a shoot-through concern due to the Miller effect. A bipolar gate drive that biases V_{gs} to a negative voltage upon turn-off is a typical solution. This application note discusses two types of bipolar gate drive circuits: the switched-capacitor circuit and the split-rail circuit.

Need for a negative V_{gs}

Similar to MOSFETs, enhancement mode GaN HEMTs with a p-type gate structure, especially the Schottky type, can be turned on unintentionally due to the Miller effect when drain-source voltage V_{ds} undergoes a large and rapid transition. This can cause excessive switching losses or even catastrophic failure in a hard-switched circuit, where the simultaneous ON of two GaN HEMTs will result in a short circuit known as shoot-through. Due to parasitic inductance, the external gate drive that clamps the gate low during OFF time cannot provide low enough impedance to prevent V_{gs} from rising, and that momentary rise may mean V_{gs} going above the gate turn-on threshold V_{gs_th} .

As an example, Figure 1 shows an oscilloscope screenshot captured during buck-mode operation of the evaluation board for ROHM's 650V GNP2050TD HEMT. The board uses a half-bridge configuration consisting of a high-side HEMT and a low-side HEMT. The input voltage is 400V. The gate pull-up resistor of the high-side HEMT is 10Ω , and the gate pull-down resistor of the low-side HEMT is 0Ω . The instantaneous inductor current is 8.2A positive. The dark-blue trace at the top is the low-side gate-source voltage V_{gs_ls} , measured with a TIVH08 IsoVu probe. The pink trace at the bottom is the low-side drain-source voltage V_{ds_ls} . As shown in the figure, V_{gs_ls} goes low first, turning off the low-side HEMT. Since the high-side HEMT isn't on yet, the 8.2A inductor current continues to flow from source to drain of the low-side HEMT. After a 120ns dead time, the high-side HEMT turns on and V_{ds_ls} rises rapidly toward 400V. As a result, V_{gs_ls} undergoes a transient (circled in red in the figure), and exhibits a positive excursion of about 3.5V.

To prevent V_{gs} from exceeding V_{gs_th} during such an event,

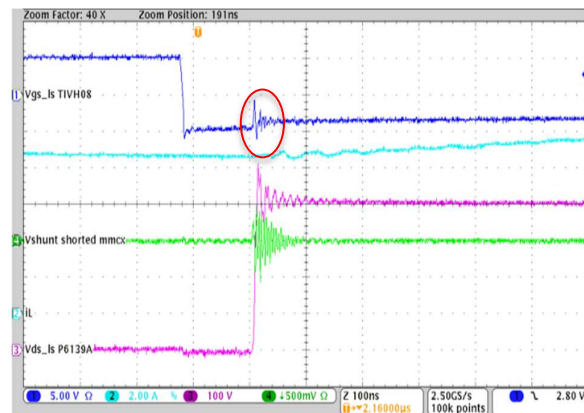
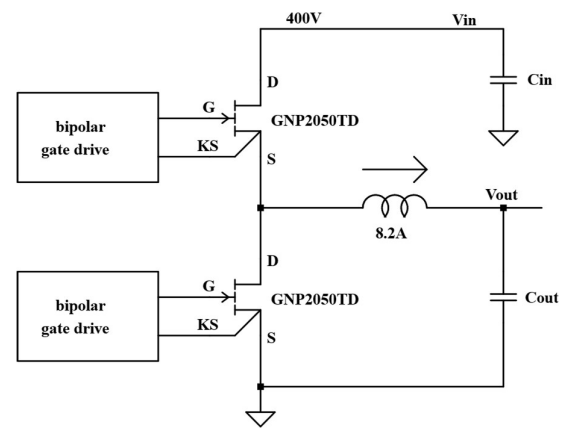


Figure 1. High-side turn-on causing low-side gate transient

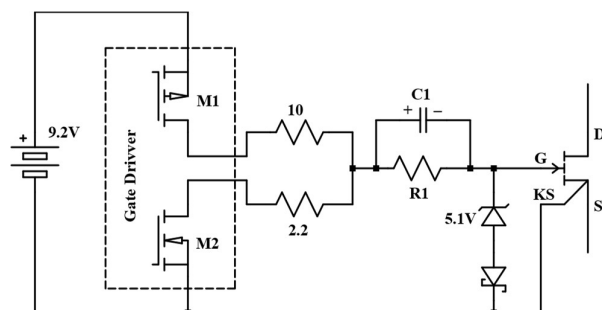


Figure 2. The switched-capacitor bipolar gate drive

V_{gs} is biased to a negative voltage upon device turn-off. In this case, V_{gs_ls} is sitting at -4V right when the high-side HEMT turns on. That is, we need to use a bipolar gate circuit that drives V_{gs} positive during ON time and negative during OFF time. Two types of bipolar gate drive circuits are commonly used: the switched-capacitor circuit and the split-rail circuit.

The switched-capacitor circuit

See Figure 2. The secondary side of the gate driver IC is typically powered by a 9.2V power supply that references the HEMT's source node. During ON time, M2 is open and M1 is closed. The Zener-Schottky branch clamps V_{gs} to $5.1V + 0.3V = 5.4V$ while C1 is being charged to $9.2V - 5.4V = 3.8V$. During OFF time, M1 is open and M2 is closed. C1 pulls charge away from the gate until V_{gs} is close to -3.8V. The gate drive is therefore bipolar.

There are several considerations here. First, resistor R1 is there to provide a DC current path during ON time to keep the Zener in breakdown state so that V_{gs} stays at the desired voltage after the initial transient and does not decay. If the chosen Zener current is 10mA, R1 will be $3.8V/10mA = 380\Omega$, or 383Ω if we use 1% resistors.

Next, if C1 is too small, it may be discharged too much by the gate to bring V_{gs} down to a voltage near -3.8V. If C1 is too large, it may not be charged sufficiently (3.8V) during the first few switching cycles, resulting in insufficiently negative V_{gs} and an increased risk of shoot-through. This is especially true if ON time is much shorter at the beginning, such as during the soft start of certain converter topologies, or during recovery from a fault.

To look at a specific case, let's use ROHM's 650V GNP3050TD GaN HEMT as an example. Assume C1 voltage drops from 3.8V to a value V_x upon turn-off. The amount of charge C1 loses during that time is therefore $Q1 = (3.8V - V_x) \cdot C1$, assuming C1 is constant vs bias voltage. Since charge lost through R1 during this short transition is negligible, charge Q1 is the same as charge Q2 coming from the gate as V_{gs} moves from 5.4V down to $-V_x$. Q2 has two parts. The first part is charge removed when V_{gs} drops from 5.4V to 0V. Per datasheet V_{gs} vs Q_g curve, this charge is 3.8nC, assuming V_{ds} rises from 0V to 400V and drain current is 10A. The second part is charge from the gate when V_{gs} drops from 0V to $-V_x$. This charge is $V_x \cdot C_{iss}$. Per datasheet, C_{iss} is 179pF. Therefore, $Q2 = 3.8nC + V_x \cdot 179pF$. Since $Q1 = Q2$, we're

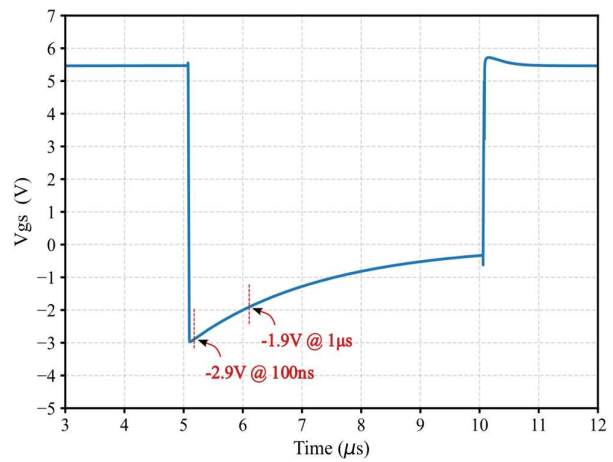


Figure 3. V_{gs} in steady state with $C1=5.6nF$ and $R1=383\Omega$

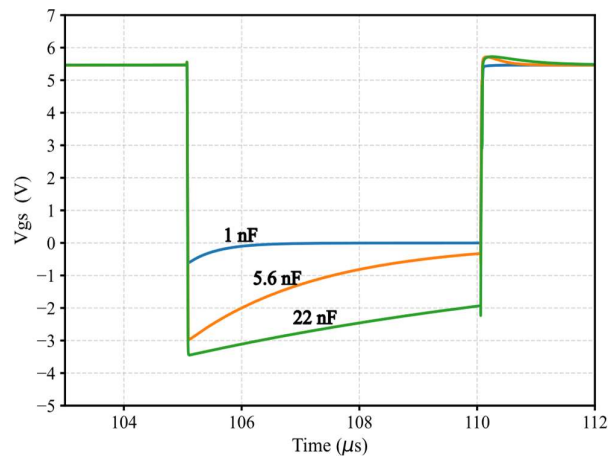


Figure 4. V_{gs} of GNP3050TD with different C1 values: 1nF, 5.6nF, and 22nF. $R1=383\Omega$.

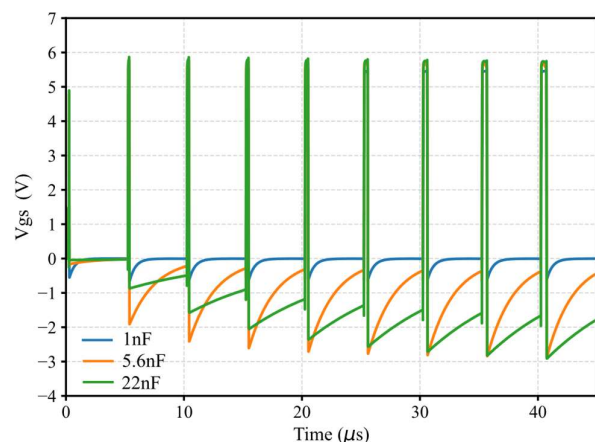


Figure 5. V_{gs} at the beginning of soft start with $C1=1nF$, 5.6nF and 22nF. $R1=383\Omega$.

going to have the following equation:

$$(3.8V - V_x) \cdot C1 = 3.8nC + V_x \cdot 179pF$$

Solving for V_x with $C1 = 5.6\text{nF}$ gives $V_x = 3.0\text{V}$.

During the rest of OFF time, $C1$ is further discharged by $R1$ in a more gradual manner. The time constant of the discharging is $383\Omega \times 5.6\text{nF} = 2.1\mu\text{s}$. The simulated V_{GS} waveform in shows this case with an OFF time of $5\mu\text{s}$. We see that V_{GS} falls to -3.0V instead of -3.8V due to loss of charge in the 5.6nF $C1$, and then decays toward 0V due to the 383Ω $R1$.

As mentioned at the beginning, the critical instant when a negative V_{GS} is actually needed is when forced commutation occurs, at the end of dead time. If the dead time between the two HEMTs is 100ns , then the decay in V_{GS} magnitude during dead time is small. Theoretically, V_{GS} retains

$$e^{-\frac{0.1\mu\text{s}}{2.1\mu\text{s}}} = 95\%$$

of its initial value of -3.0V , which is -2.9V . As dead time increases however, this may eventually become a concern. For example, if the dead time is $1\mu\text{s}$, V_{GS} will be -1.9V only.

$C1$ can always be increased to mitigate this concern. shows V_{GS} under different $C1$ values. The larger $C1$ is, the closer V_{GS} will be to -3.8V upon turn-off, and the more slowly V_{GS} will decay toward 0V . The trade-off is that $C1$ initially takes longer to fully charge. In the Figure 2 circuit, the time constant for charging up $C1$ is $10\Omega \times 5.6\text{nF} = 56\text{ns}$. If $C1$ increases to 20nF , that time constant will be 200ns . We need to make sure that startups and transients are not a problem.

shows the high-side V_{GS} during the first few switching cycles of a 1ms soft start in a 100kHz buck converter, for various $C1$ values. ON time increases by 50ns per switching cycle. If $C1$ is 22nF , V_{GS} reaches -2.6V after 5 cycles whereas if $C1$ is 5.6nF , that V_{GS} value is reached after 3 cycles. If a sufficiently negative V_{GS} is necessary during even the first cycle, an alternative measure should be taken to address it. For example, to ramp the input voltage up only after toggling the gates a few times. Also note that when $C1$ is 0V to begin with, the charging current during the first few cycles can be higher than normal, depending on the ON time. That can cause positive V_{GS} to exceed the normal value by some amount because the Zener needs to absorb a current that's much higher than the normal breakdown value. Make sure positive V_{GS} during the first few cycles does not exceed the absolute maximum. If the 10Ω connected to M1 (Figure 2) is to be reduced, keep in mind that this effect will be more prominent.

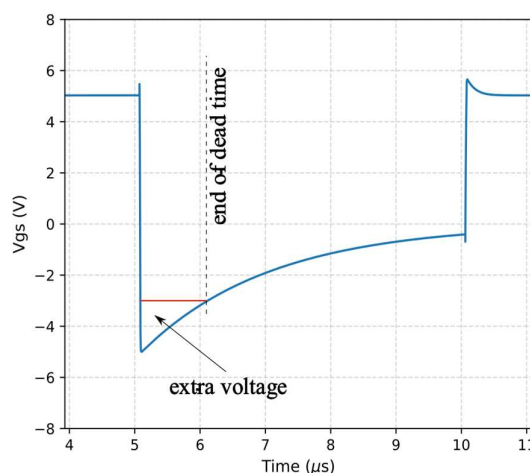


Figure 6. Extra loss due to exponential waveform

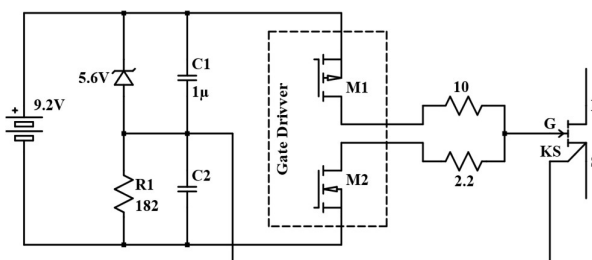


Figure 7. Split-rail bipolar gate drive circuit

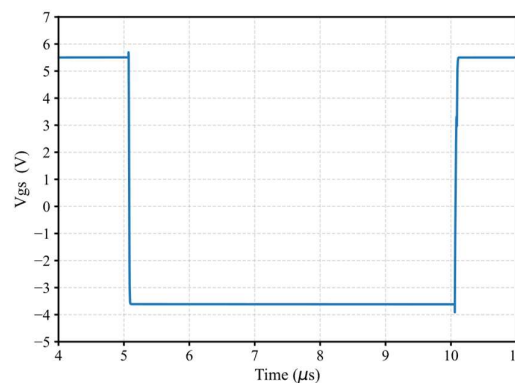


Figure 8. V_{GS} in steady state, split-rail gate drive

Another consideration related to the exponentially decaying V_{GS} during OFF time, especially if the dead time is long, is that the waveform causes an unnecessary conduction loss during dead time. illustrates the idea. Suppose V_{GS} initially falls to -5V and the time constant of the decay is $2.25\mu\text{s}$. If dead time is $1\mu\text{s}$, V_{GS} will be

$$-5\text{V} \cdot e^{-\frac{1\mu\text{s}}{2.25\mu\text{s}}} = -3.2\text{V}$$

Further assuming this -3.2V is the target V_{gs} at the end of the dead time, compared to a constant V_{gs} of -3.2V (red horizontal line in the figure), the triangular area indicated by the arrow has extra V_{gs} that's unnecessary. This extra V_{gs} increases V_{sd} by approximately the same amount, resulting in additional conduction loss during freewheeling. For example, if the freewheeling current is 10A and switching frequency is 100kHz, the extra loss will be roughly $(5V-3.2V)/2 \times 10A \times 1\mu s/10\mu s = 0.9W$.

It might also be of interest to find out how high C1 needs to be when driving the GNP3018TF, a beefier 18mΩ 650V GaN HEMT. Again, like the GNP3050TD case, assume C1 voltage drops from 3.8V to 3.0V upon turn-off. Per datasheet, charge coming from the gate while V_{gs} falls from 5V to 0V is 11nC. C_{iss} is 434pF. Like the previous case, we then have

$$(3.8V - 3.0V) \cdot C1 = 11nC + 3.0V \cdot 434pF$$

That is, $C1 = 15nF$. This is about 3 times the 5.6nF required by the GNP3050TD. With this much C1, the initial settling time will be similar to that of $C1 = 22nF$ as shown in .

A quick examination of the equation above reveals that in general, C1 value is approximately proportional to the total gate charge of the GaN HEMT being driven.

The split-rail circuit

One implementation of the split-rail circuit is shown in . Here, the same 9.2V supply is connected to the secondary side of the driver as in the first method, but a midpoint voltage is created and used as the source-node reference. As the gate switches between the positive and negative terminals of the 9.2V supply, V_{gs} is either charged up to the 5.6V Zener voltage or discharged to $-(9.2V-5.6V) = -3.6V$. The V_{gs} waveform for a converter with a 5μs OFF time is shown in . The positive V_{gs} level is set by the 5.6V Zener voltage, while the negative V_{gs} level is determined by the voltage across C2.

Capacitors C1 and C2 smooth out the pulsating gate current and ensure that the Zener's current is largely DC. The required capacitance values can be estimated as follows. Assuming the HEMT is ROHM's GNP3050TD. If V_{ds} toggles between 400V and 0V, and V_{gs} is charged up to 5.6V during ON time, per datasheet curve, total gate charge is 4.1nC. Assuming a switching frequency of 100kHz, the average gate charging current is then $4.1nC \times 100kHz = 0.41mA$. If we allow the Zener to sink 20mA under no load, that current becomes 20mA

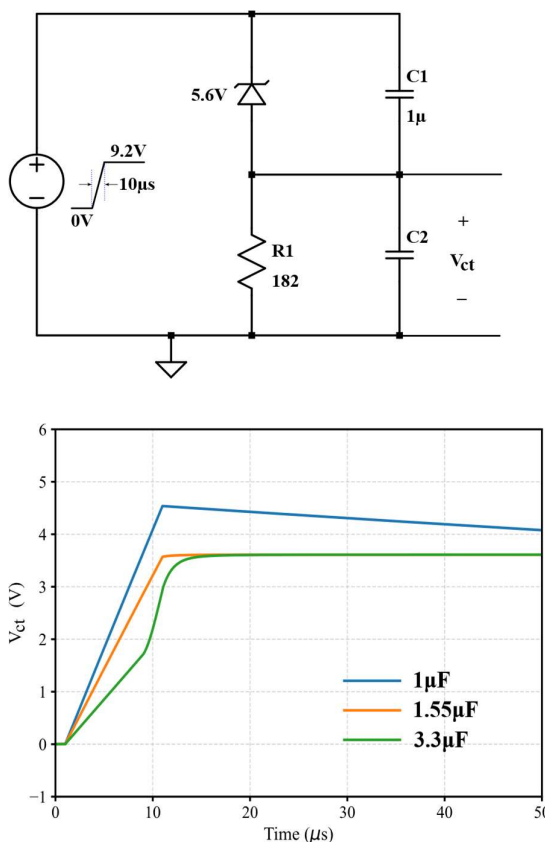


Figure 9. Settling of center-tap voltage V_{ct} with $C2 = 1\mu F$, 1.55μF and 3.3μF

- 0.41mA = 19.59mA, which is more than sufficient to maintain a stable Zener voltage. Assume we want to limit the C2 voltage drop during ON time to 10mV. The sum of C1 and C2 must therefore be at least $4.1nC/10mV = 0.41\mu F$. We can simply use 1μF for each cap.

Again, let's also check the GNP3018TF. Per datasheet, if V_{gs} is charged up to 5.6V during ON time, total gate charge is 13nC. At 100kHz switching frequency, the average gate charging current is $13nC \times 100kHz = 1.3mA$, still much lower than the 20mA Zener current. To limit the C2 voltage drop during ON time to 10mV, the sum of C1 and C2 must be at least $13nC/10mV = 1.3\mu F$. Again, we can simply use 1μF for each cap.

The dynamic characteristic of the split-rail circuit is of interest because we don't want to see a situation where V_{gs} goes outside of its limits even momentarily. For example, assume that the 9.2V rail ramps up within 10μs during startup. If we use 1μF for each of the caps, the center tap will initially be sitting at 4.6V with regard to the negative terminal of the 9.2V supply. That is, exactly in the middle. As the center-tap voltage V_{ct} moves toward the final 3.6V, R1 discharges C2, and the

Zener current will start to increase, until it finally equals $R1$ current. How fast is the settling? We know that the time constant formed by $R1$ and $C1+C2$ is $R1 \times (C1+C2)$. In our case, it is $182\Omega \times 2\mu F = 364\mu s$. How fast the settling depends on the difference between the initial voltage and the final voltage as well as the time constant. That is, the center-tap voltage V_{ct} is

$$3.6V + (4.6V - 3.6V) \cdot e^{-\frac{t}{364\mu s}}$$

This equation is for the case when V_{ct} is higher than 3.6V initially. shows three scenarios based on three different values of $C2$. We see that when $C2 = 1.55\mu F$, there is no settling time. This is because $1.55\mu F / 1\mu F = 1.55 = 5.6V / 3.6V$. In general, we want the ratio of the capacitances to equal the reciprocal of the ratio of their steady state voltages. In reality, it is tough to guarantee such a capacitance ratio with MLCCs due to tolerance, mismatch in tempco and in C-Vbias characteristic. However, as can be seen in the figure, if $C2$ is larger than the perfect value of $1.55\mu F$, settling time is far shorter than if $C2$ is smaller than $1.55\mu F$. This is because in the former case V_{ct} will be lower than 3.6V to begin with, and the Zener will break down and quickly bring V_{ct} up to 3.6V.

To avoid the initial center-tap voltage issue, either size $C2$ such that $C2/C1$ is no less than $5.6V/3.6V$, or wait for the voltage to settle before startup, or ramp up the 9.2V supply slowly so that V_{ct} does not significantly overshoot or undershoot.

Summary

This application note discusses two bipolar gate drive circuits. The switched-capacitor circuit establishes a decaying negative gate voltage upon turn-off, whereas the split-rail circuit creates nearly DC positive and negative gate-drive rails from a single-ended supply. Both circuits may need to address the initial settling issue, but the mitigation strategies are different. The switched-capacitor circuit is more sensitive to extreme transients where ON time shrinks significantly. The split-rail circuit can only be used with a secondary-side power rail whose center tap is allowed to connect to the source of the HEMT.

Figure 10 and Figure 11 show half-bridge implementations using the two bipolar gate drive circuits discussed here, with ROHM's GaN HEMTs, isolated drivers, and LDOs.

Note in Figure 10 a 5.1V Zener is used at the gate but in Figure 11 a 5.6V Zener is used instead. This is because in Figure 10, the switched-capacitor circuit requires a Schottky to be in series with the Zener to prevent the negative V_{gs} from being clamped by the Zener. The Zener-Schottky branch has a breakdown voltage of about $5.1V + 0.3V = 5.4V$, close to the 5.6V in Figure 11.

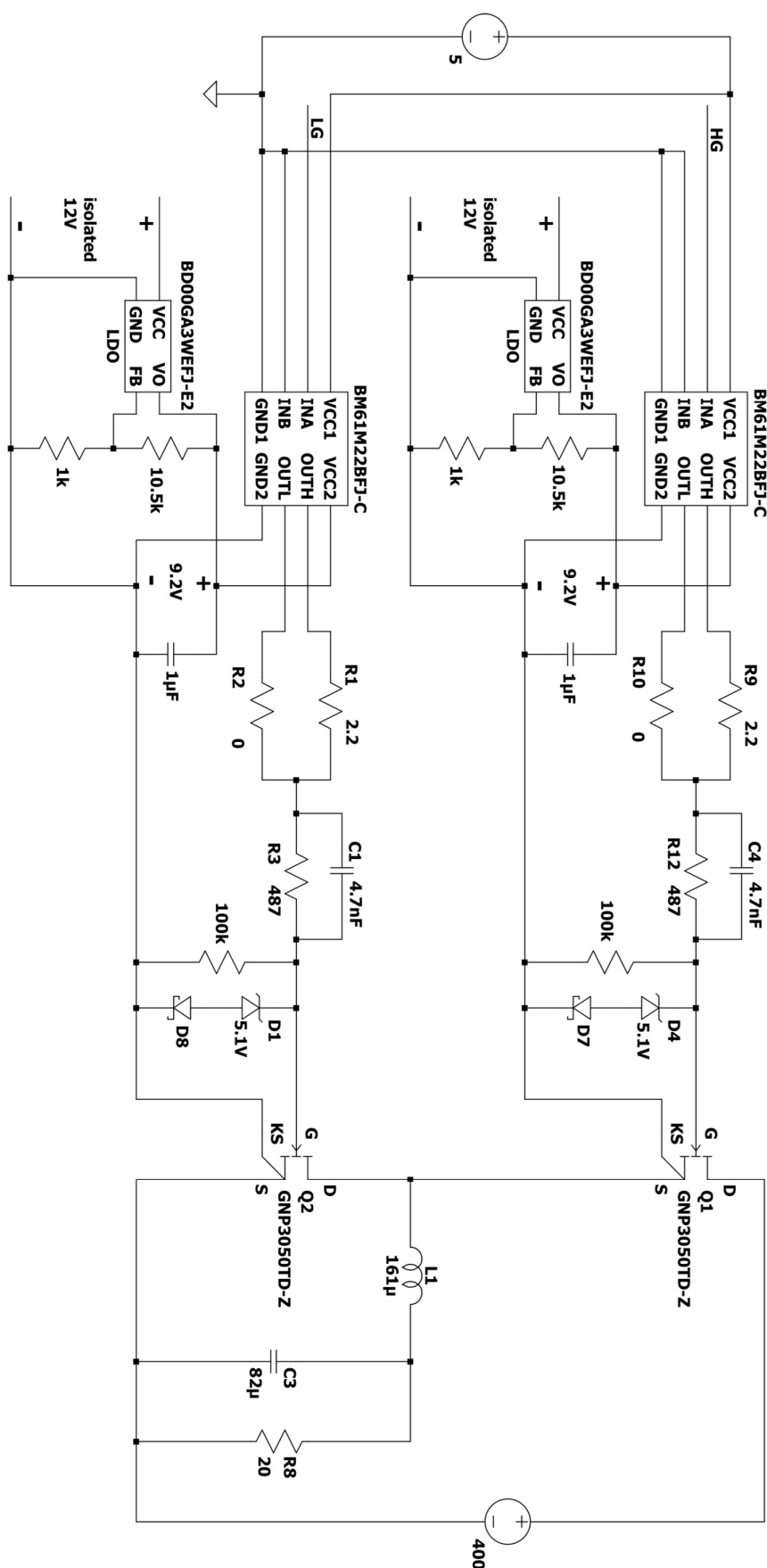


Figure 10. Switched-capacitor bipolar gate drives in a half bridge



History and author

August 2026	Rev.001	Dongbing Zhang
October 2026	Rev.002	Dongbing Zhang

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