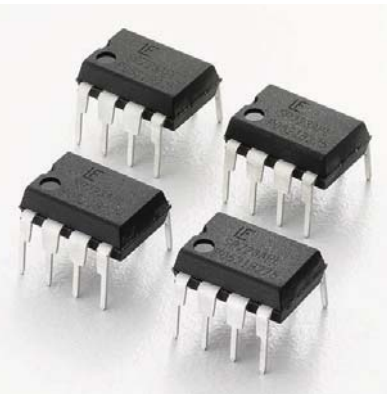
Littelfuse®

Expertise Applied | Answers Delivered



PRODUCT CATALOG & DESIGN GUIDE

SPAs

Silicon Protection Array (SPA) Products

Littelfuse Circuit Prot
Solutions Portf

Consumer Electronics | Telecom | White Goods | Medical Equipment | TVSS and Power S

DESIGN SUPPORT

Live Application Design and Technical Support—Tap into our expertise. Littelfuse engineers are available around the world to help you address design challenges and develop unique, customized solutions for your products.

Product Sampling Programs—Most of our products are available as samples for testing and verification within your circuit design. Visit Littelfuse.com or contact a Littelfuse product representative for additional information.

Product Evaluation Labs and Services—Littelfuse global labs are the hub of our new product development initiatives, and also provide design and compliance support testing as an added-value to our customers.

OVERVOLTAGE SUPPRESSION TECHNOLOGIES (1-6)

1. TVS Diodes — Suppress overvoltage transients such as Electrical Fast Transients (EFT), inductive load switching and lightning in a wide variety of applications in the computer, industrial, telecom and automotive markets.

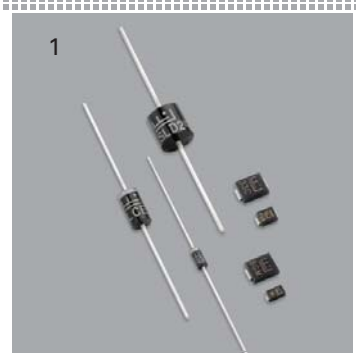
2. Varistors — Multiple forms, from Metal Oxide Varistors (MOVs) that suppress transient voltages to Multi-Layer Varistors (MLVs) designed for applications requiring protection from various transients in computers and handheld devices as well as industrial and automotive applications.

3. SIDACtor® Devices— Complete line of protection thyristor products specifically designed to suppress overvoltage transients in a broad range of telecom and datacom applications.

4. Gas Plasma Arrestors (GDTs) — Available in small footprint leaded and surface mount configurations, Littelfuse GDTs respond fast to transient overvoltage events, reducing the risk of equipment damage.

5. Silicon Protection Arrays — Designed specifically to protect analog and digital signal lines from electrostatic discharge (ESD) and other overvoltage transients.

6. PulseGuard® ESD Suppressors — Available in various surface mount form factors to protect high-speed digital lines without causing signal distortion.



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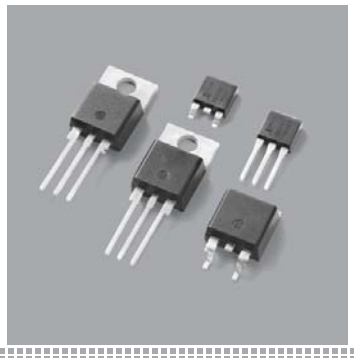
Supplies | Lighting | General Electronics

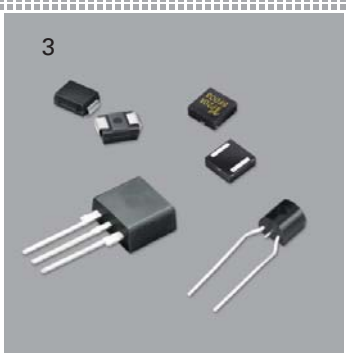
SWITCHING TECHNOLOGIES

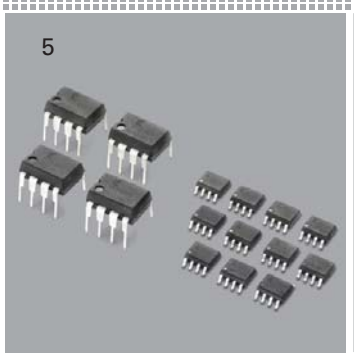
Switching Thyristors— Solid-state switches used to control the flow of electrical current in applications, capable of withstanding rated blocking/off-state voltage until triggered to on-state.

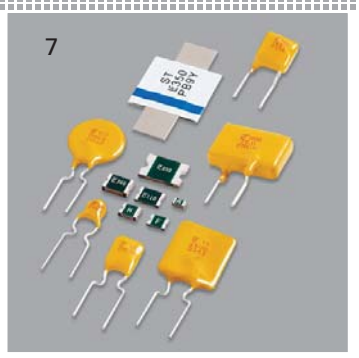
ACCESSORIES

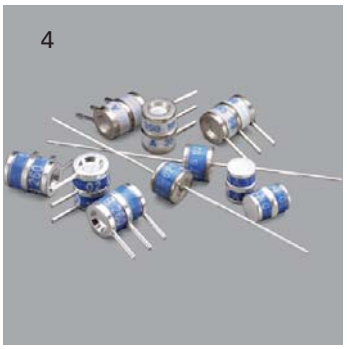
In addition to our broad portfolio of circuit protection technologies, we offer an array of **fuse holders** including circuit board, panel or in-line wire mounted devices to support a wide range of application requirements.

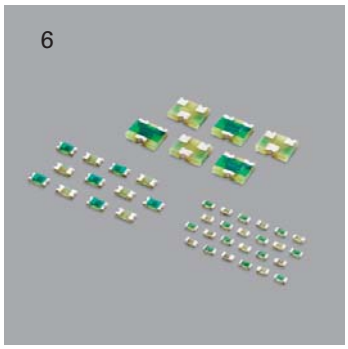












OVERCURRENT PROTECTION TECHNOLOGIES (7-8)

7. Positive Temperature Coefficient Devices (PTCs)— Provide resettable overcurrent protection for a wide range of applications.

8. Fuses — Full range including surface mount, axial, glass or ceramic, thin-film or Nano$^{2®}$ style, fast-acting or SloBlo®, MINI® and ATO® fuses.

www.littelfuse.com for more information.











Circuit Protection with Silicon Protection Arrays (SPAs)

Littesfuse SPAs are designed to protect electronics from very fast and often damaging voltage transients, such as lightning and electrostatic discharge (ESD). They offer an ideal protection solution for I/O interfaces and digital and analog signal lines, in computer and consumer portable electronics markets.

Littelfuse SPAs are available in a range of surface mount and through hole (PDIP) package configurations, including SC70, SOT23, SOT143, TSSOP-8 MSOP-8, DIP, and SOIC.

Features

- Low capacitance of 30pF to 0.65pF typically
- High level of protection: ESD IEC 610000-4-2 contact discharge up to ±30kV, air discharge up to ±30kV, EFT IEC 61000-4-4 40A (5/50ns)
- Low clamping voltage
- Up to 14 inputs protection
- Space saving arrays, ultra small packages available
- ROHS compliant
- Pb-Free and Halide-free designs available

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Product Selection Table

Technology	SCR Array					TVS Array			Diode Array					
Series	SP720	SP721	SP723	SP724	SP725	SP05	SP1001	SP1002	SP3001	SP3002	SP3003	SP3004	SP03-6	SPUSB1
Surface Mount Packages	PDIP SOIC	PDIP SOIC	PDIP SOIC	SOT23	SOIC	SC70 SOT23 SOT143 TSSOP MSOP	SC70 SOT553 SOT563	SC70	SC70	SC70	SC70-5, SC70-6, SOT553, SOT563, MSOP10	SOT563	SOIC	SC70
Working Voltage	2-30V	2-30V	2-30V	1-20V	2-30V	5.5V	6V	6.5V	6V	6V	6V	6V	5V	5.5V
Capacitance	3pF	3pF	5pF	3pF	5pF	30pF	8pF	5pF	0.65pF	0.85pF	0.65pF	0.85pF	16pF	47pF
Number of Channels	14	6	6	4	4	2,3,4,5,6	2,4,5	1	4	4	2,4	4	2	1
ESD Rating (Contact Discharge, IEC61000-4-2)	4kV	4kV	8kV	8kV	8kV	20kV	8kV	8kV	8kV	12kV	8kV	12kV	8kV	15kV
VCLAMP (8/20)							8.0V @ 1A	9.2V @ 1A	9.5V @ 1A	9.5V @ 1A	10.0V @ 1A	10.0V @ 1A	20V @ 100A	
8/20 Rating	3A	3A	7A	3A	14A		2A	2A	2.5 A	4.5 A	2.5 A	4 A	150 A	
RoHS	Yes													

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RoHS Pb SP720 Lead-Free/Green Series	57
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Overvoltage Suppression Facts

Transient Threats – What Are Transients?

Voltage Transients are defined as short duration surges of electrical energy and are the result of the sudden release of energy previously stored or induced by other means, such as heavy inductive loads or lightning. In electrical or electronic circuits, this energy can be released in a predictable manner via controlled switching actions, or randomly induced into a circuit from external sources.

Repeatable transients are frequently caused by the operation of motors, generators, or the switching of reactive circuit components. Random transients, on the other hand, are often caused by Lightning and Electrostatic Discharge (ESD). Lightning and ESD generally occur unpredictably, and may require elaborate monitoring to be accurately measured, especially if induced at the circuit board level. Numerous electronics standards groups have analyzed transient voltage occurrences using accepted monitoring or testing methods. The key characteristics of several transients are shown in the table below.

	VOLTAGE	CURRENT	RISE-TIME	DURATION
Lighting	25kV	20kA	10 µs	1ms
Switching	600V	500A	50µs	500ms
EMP	1kV	10A	20ns	1ms
ESD	8kV	30A	<1ns	100ns

Table 1. Examples of transient sources and magnitude

Characteristics of Transient Voltage Spikes

Transient voltage spikes generally exhibit a "double exponential" wave, as shown below for lightning and ESD.

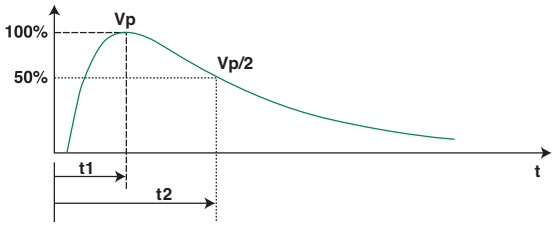


Figure 1. Lightning Transient Waveform

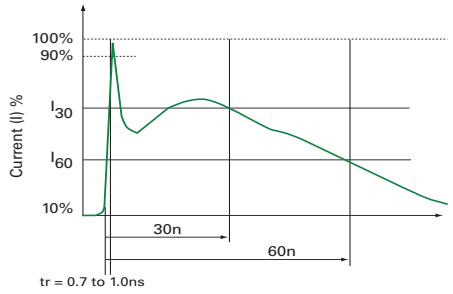


Figure 2. ESD Test Waveform

The exponential rise time of lightning is in the range 1.2µsec to 10µsec (essentially 10% to 90%) and the duration is in the range of 50µsec to 1000µsec (50% of peak values). ESD on the other hand, is a much shorter duration event. The rise time has been characterized at less than 1.0ns. The overall duration is approximately 100ns.

Why are Transients of Increasing Concern?

Component miniaturization has resulted in increased sensitivity to electrical stresses. Microprocessors for example, have structures and conductive paths which are unable to handle high currents from ESD transients. Such components operate at very low voltages, so voltage disturbances must be controlled to prevent device interruption and latent or catastrophic failures.

Sensitive microprocessors are prevelant today in a wide range of devices. Everything from home appliances, such as dishwashers, to industrial controls and even toys use microprocessors to improve functionality and efficiency.

Most vehicles now also employ multiple electronic systems to control the engine, climate, braking and, in some cases, steering, traction and safety systems.

Many of the sub- or supporting components (such as electric motors or accessories) within appliances and automobiles present transient threats to the entire system.

Careful circuit design should not only factor environmental scenarios but also the potential effects of these related components. Table 2 below shows the vulnerability of various component technologies.

Device Type	Vulnerability (volts)
VMOS	30-1800
MOSFET	100-200
GaAsFET	100-300
EPROM	100
JFET	140-7000
CMOS	250-3000
Schottky Diodes	300-2500
Bipolar Transistors	380-7000
SCR	680-1000

Table 2: Range of device vulnerability.

Transient Voltage Scenarios

Electrostatic Discharge (ESD)

Electrostatic discharge is characterized by very fast rise times and very high peak voltages and currents. This energy is the result of an imbalance of positive and negative charges between objects.

ESD that is generated by everyday activities can far surpass the vulnerability threshold of standard semiconductor technologies. Following are a few examples:

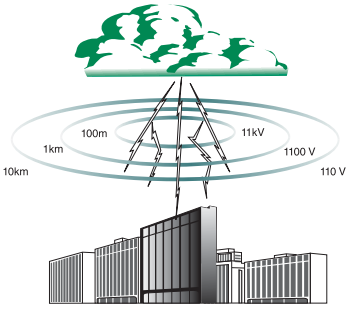
- **Walking across a carpet:**
  35kV @ RH = 20%;1.5kV @ RH = 65%
- **Walking across a vinyl floor:**
  12kV @ RH = 20%;250V @ RH = 65%
- **Worker at a bench:**
  6kV @ RH = 20%;100V @ RH = 65%
- **Vinyl envelopes:**
  7kV @ RH = 20%;600V @ RH = 65%
- **Poly bag picked up from desk:**
  20kV @ RH = 20%;1.2kV @ RH = 65%

Lightning Induced Transients

Even though a direct strike is clearly destructive, transients induced by lightning are not the result of a direct strike.

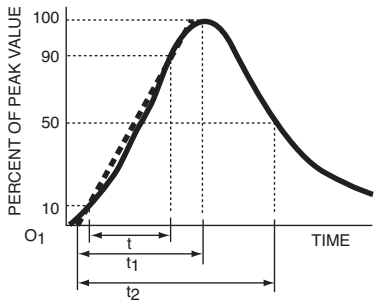
When a lightning strike occurs, the event creates a magnetic field which can induce transients of large magnitude in nearby electrical cables.

A cloud-to-cloud strike will effect not only overhead cables, but also buried cables. Even a strike 1 mile distant (1.6km) can generate 70 volts in electrical cables.



In a cloud-to-ground strike (as shown at right) the transient-generating effect is far greater.

This diagram shows a typical current waveform for induced lightning disturbances.



Switching

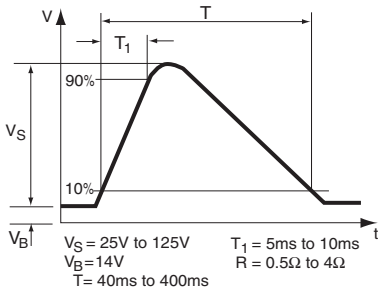
The switching of inductive loads generates high energy transients which increase in magnitude with increasingly heavy loads. When the inductive load is switched off, the collapsing magnetic field is converted into electrical energy which takes the form of a double exponential transient. Depending on the source, these transients can be as large as hundreds of volts and hundreds of Amps, with duration times of 400 milliseconds.

Typical sources of inductive transients include:

- **Generator • Motor**
- **Relay**
- **Transformer**

These examples are common in electrical and electronic systems. Because the sizes of the loads vary according to the application, the wave shape, duration, peak current and peak voltage are all variables which exist in real world transients. Once these variables can be approximated, a suitable suppressor technology can be selected.

The diagram at right shows a transient which is the result of stored energy within the alternator of an automobile charging system.



A similar transient can also be caused by other DC motors in a vehicle. For example, DC motors power amenities such as power locks, seats and windows. These various applications of a DC motor can produce transients that are just as harmful to the sensitive electronic components as transients created in the external environment.

Transient Voltage Suppression Factors and Techniques

Why Implement Circuit Protection?

It is important to consider that most electronic equipment will spend 99% of its useful life in environments where it is subject to ESD.

ESD can be generated from a wide range of everyday factors such as very dry air, static from plastics, or walking across a floor or carpet, and can be present during every phase of useful life from manufacturing, to product shipping, receiving, to field handling.

Electrostatic Discharge (ESD) causes millions of dollars worth of damage to electrical components, rendering circuit boards non-functional, and corrupting or erasing vital data. Often the damage is not detectable until a malfunction occurs. That could take weeks, months, or even years before an unpredictable and premature breakdown causes a field failure.

If you use electronic components or boards in your products, adding devices that suppress ESD damage can result in preventing damage to your company reputation and bottom line. Other tangible benefits include:

- Higher manufacturing yields
- Less rework and inventory
- Reduced overall costs
- Fewer field failures and warranty calls
- Increased product reliability
- More repeat business

Companies can also face legal liabilities if the product fails due to ESD/Transient damage. So it is important to include ESD/Transient Immunity in all phases of the project.

It is wise to factor Electrostatic Discharge (ESD) Immunity strategies early in design processes. If a device in development fails ESD immunity tests–the scramble to avoid complete redesign often leads to higher parts cost and more manual assembly during manufacturing.

There is little time to fully analyze which components do and do not provide ESD immunity. Worse, under pressure, finding comprehensive information tailored to ESD immunity design is very difficult, leaving your product vulnerable to ESD/Transient damage.

Littelfuse associates can help you address these challenges, offering extensive application expertise and product testing capabilities. Please contact your local Littelfuse representative for assistance.

ESD Electrical Characteristics

ESD, in contrast to switching and surge transients, has a very short transition from zero to maximum current and voltage. The rise time of an ESD event is less than 1 nanosecond (1ns), while the other transients take longer than 1 microsecond (1µs) to reach their peaks.

The International Electrotechnical Commission (IEC) has developed a model of the human-generated ESD event. This model is used in the IEC's test specification for determining if systems (computers, networks, cell phones, set top boxes, etc.) are susceptible to ESD events. The test specification quantifies the methodology for introducing ESD into the system as well as the various voltage and current levels that define the ESD event.

While these circuits have typical maximum ESD protection levels of 2,000V, humans can generate ESD voltages in excess of 15,000V. This level of ESD is in excess of the on-chip protection circuits and can damage them.

Common ESD Damage

A transient discharged into an electronic system creates three general types of adverse effects:

1. Soft Failures/Data Corruption: can occur to a part of the data stream, or the system may latch up. This is a temporary problem and is solved by data correction (for data corruption) or by re-booting the system (for latch up).

2. Latent Defects: A component might be partially degraded, but able to function properly. Typically a latent defect may cause a system to fail prematurely.

3. Catastrophic Failures: An internal component is rendered inoperable, and cannot function properly. This is a permanent condition. In the case of **Junction Burnout**, a short circuit condition is created in a transistor of the circuit. The metallic interconnect (Trace Line) is "pulled through" one of the semiconductor layers (Alloy Spike) or one of the semi conducting junctions is directly short circuited (Junction Short). In **Oxide Punch-Through**, the metallic interconnect is "pulled through" the oxide layer to provide a short circuit on the signal line. In **Metallization Burnout**, the metallic interconnect is melted, much like a fuse. It creates an open circuit condition on the signal line.

The use of ESD circuit protection components like Littelfuse SPAs will help you avoid such problems.

Common ESD Entry Points

ESD can quickly finds weak spot(s) and sneak into devices using a wide range of potential coupling paths. Careful consideratation about potential weak points, and taking steps to seal off those paths and fortify the most vulnerable electronic components is vital.

Below are potential ways an ESD pulse can enter an electronic device:

1. An initial electric field from an arc can capacitively couple over a large surface area. It can appear like a signal to high-impedance analog circuits and measure up to 4000 V/m 100 mm

2. Current or charge from the arc can be injected and:

- Smash through insulating layers in the component and damage the gates of MOSFETs and CMOS devices
- Trigger a latch-up in CMOS devices
- Short circuit reverse and forward-biased PN junctions
- Melt bonding wires

3. A voltage pulse on conductors caused by current (V = L * dI/dt) whether from ground, power or signal wiring, can spread into every device that is linked;

4. An intense magnetic field emitted from an ESD arc can have a frequency range of 1 to 500Mhz, which can inductively couple into every nearby wiring loop and be as high as 15 A/m 100 mm

5. An electro-magnetic field generated by the arc's magnetic field can radiate and couple into long wires that act like receiving antennas

ESD Suppression Strategies

Chip Level ESD Protection

In the heart of the device is the integrated circuitry (IC) responsible for its processing and communication function.

Typically, trade-offs for the chip designer are ESD protection versus die space and the demand of smaller and faster chips-which require sub-micron processes and very fine line widths. As more ESD protection structures are incorporated into the chip, survivability increases. The choice is either less space available for functional circuitry or make the chip larger.

In today's market, "smaller and faster" is the goal, and ESD protection is sacraficed for more on-chip space to boost functionality and speed. Consequently, circuits will become more sensitive to ESD and other transients.

Input and output port connections allow the free flow of data – including transients. ESD can enter a port–or the disconnected end of the cable while connecting/disconnecting cables. It will then travel through the connector to the PC board and propagate down the data lines toward the ICs.

Littelfuse offers small size PSA packages to provide maximum protection with a minimum of space. The suppressor devices are installed between the data line and the chassis ground (parallel connection) and shunt the ESD transient from the data line to the ground. Optimally, SPAs should be the first thing a transient should encounter on the board.

NOTE: For high-speed signal pins, devices with extremely low capacitance levels should be used. Consult www.littelfuse.com for more detailed information on which products offer best protection for high-speed connectors.

Board Level ESD Protection

Especially critical in portable systems is the board layout. Parasitic inductance in the protection path can result in significant voltage overshoot, easily getting past the insulation barriers and damaging the the circuit. This is especially critical in the case of fast rise-time transients such as ESD or EFT. However, the need for board-level protection will vary from system to system.

Factors determining level of need:

- The board layout
- ESD capabilities of the IC
- Physical ability of ESD transients to get on the data lines

Empirical testing can also be done to help determine the system's susceptibility.

(section continued on next page)

Supplemental ESD Protection

When deciding on more ESD protection, the next step is to identify the appropriate suppressor. Consider the following specifications to make an appropriate selection:

- Capacitance
- Peak voltage and clamping level
- Leakage current
- System operating voltage
- Number of lines to be protected

Capacitance is becoming an extremely important criterion since the data rates at which electronic products are communicating continue to increase. As previously mentioned, the **Clamping Level** of the suppressor determines how much of the ESD transient is eliminated. A related value is the **Peak Voltage.** As the suppressor transitions from high to low resistance, a portion of the ESD wave front is transmitted before the clamping voltage is established. These are important factors for those IC's that do not have a substantial amount of on-chip ESD protection. In this case, it is important that as little ESD as possible is actually experienced by the IC. For these circuits, the SP050x and SP72x product lines are ideal. They have extremely low peak and clamping voltages to provide ultimate protection to the IC.

Leakage Current is the amount of current passed through the suppressor as the circuit operates normally (i.e. at rated voltage). It is an important consideration for applications where the main power supply is battery-driven. In these cases, the suppressor should allow as little leakage as possible, to avoid increasing the battery drainage time.

All Littelfuse ESD suppressors have very low typical leakage current. Suppressors have varied **System Operating Voltage** specifications determined by their construction. This is used to determine if the part is suitable for given circuit parameters. For example, a 5 VDC-rated part should not be used where the ESD reference is a 9 VDC bus. The excess voltage may cause degradation of the part.

Another consideration is the **Number Of Lines To Be Protected.** This is determined by the system's data protocol. For example, USB buses have two data lines, RS 485 uses two lines per differential pair, 10/100 BaseT Ethernet uses four lines, etc. In cases where multiple data lines will be protected, it may be desirable to use a multi-line suppressor to save board space and installation costs. Littelfuse suppressors are available in single and multiple line packages to offer a broad selection of high quality SPAs to the circuit designer.

Suppressor Location

Place the suppressor as near the line that it is protecting as possible. ESD transient should hit the suppressor first on entry to the board. Because ESD is such a fast rise-time event, any distance between the protected line and the ESD suppressor will mean more transient voltage to the IC.

ESD Prevention During The Manufacturing Process

Manufacturers typically include structures stamped directly on the die to provide some ESD protection of the circuits through the manufacturing process. Production environments tightly control and take precautions to ensure that static electricity levels on personnel and equipment are minimized. For example, when handling parts or their containers, workers wear wrist straps, anti-static garments and work at grounded workstations. Various environmental controls (humidity/air ionization) are also implemented. Finally, by transporting products in special electrostatic shield packaging ensures safe arrival to the customer.

ESD Immunity Test Standards

To test their products, manufacturers apply one of several testing models using either the CDM (Charged Device Model), MM (Machine Model), and/or HBM (Human Body Model). More powerful transients await as the product moves outside the controlled factory environment. Often designers and/or engineers will need to provide additional off-chip, board-level solutions to fill in the gaps.

Look for Technical Briefs at www.littelfuse.com that address solutions available to reduce catastrophic failures and allow the equipment to reliably withstand user-generated ESD events, as typified in the IEC test specification 61000-4-2.

Additional Transient Immunity Considerations

Film Resistors

In-line film resistors between inputs and off-board connectors provide minimal transient protection and are often damaged themselves.

Component Quality

Active components play the biggest role towards ESD/ Transient immunity. If using substitute and/or secondary source components, test and analyze them thoroughly. Though functionally equivalent, they may lack the ESD/ Transient immunity of the preferred components.

Multi-Suppressor Combinations

ESD protection through use of Silicon Protection Arrays (SPAs) included in combination with other filters and transient suppressors is another strategy for inputs, outputs and power nets. See www.Littelfuse.com for more information.

Preventive Software Programming

The basic requirement of good software is to cleanly handle abnormal operations, no matter the cause.

Internal Moving Parts

Equipment with moving parts can become its own ESD/ Transient generator. Printers and copiers are especially susceptible because they carry paper through paper rollers and use toner. In general, the problem areas include sliding parts, rolling parts, flexing parts, flowing liquids and airflow carrying particles or liquid droplets.

Finally, once the design has been approved, it's tempting to substitute components in effort to boost product performance. Often newer chips and components are faster but more sensitive to transients causing new emissions and immunity problems. Keep fully informed, as periodically suppliers can make changes to components that may affect ESD Immunity. Test the new parts to determine if they are still effective. Planning is key, in the event the new product doesn't work or the company ceases producing it, having several backup plans will help your company face unforseen challenges.

SPA Technology Overview and Typical Applications

Introduction to Silicon Protection Arrays (SPAs)

Littelfuse Silicon Protection Arrays (SPAs) are designed to protect analog and digital signal lines, such as USB and HDMI, from various transient threats using the lowest possible clamp voltage. They offer broader application use and improved impulse protection performance over conventional diodes.

These robust diodes can safely absorb repetitive ESD strikes at the maximum level (Level 4) specified in the IEC 61000-4-2 international standard, without performance degradation.

Key Features

- Low capacitance 30pF to 0.65pF typically
- High level of protection ESD IEC 610000-4-2 contact discharge up to ±20kV, air discharge up to ±30kV, EFT IEC 61000-4-4 40A (5/50ns)
- Low clamping voltage
- Low leakage 0.5µA maximum
- Up to 14 inputs protection
- Available in space saving Surface Mount, Through-Hole and small size packages for mounting close to input ports for optimal protection
- ROHS compliant and Lead-Free

Littelfuse SPAs: How they Work?

Littelfuse Silicon Protection Arrays (SPA's), provide high level protection against ESDs, Electromagnetic Interferences (EMI), Electrical Fast Transients (EFT) and Lightning, mainly for sensitive digital and analogue input circuits, on data, signal, or control lines operating on power supplies.

SPA's work in two ways, first, they absorb transients with diodes, to steer the current, and then, an avalanching or zener diode, clamps the voltage levels. This prevents the device from exceeding its voltage rating. During over-voltage fault conditions, the device must have a low clamp voltage at the specified current wave form to protect sensitive IC's and ports.

In normal operation, the reverse stand off voltage must be higher than the equipment supply/working voltage, with low leakage current to prevent power supply loading. The device capacitance must be low enough to reduce input signal distortion. The device package must have a small footprint and low height to enable a high density Printed Circuit Board (PCB) layout.

The device must withstand multiple ESD/EFT pulses as specified in the IEC 61000-4-2.

Terms and Definitions

Operating Voltage Range (Vsupply)

The range limits of the power supply voltage that may be across the V+ and V- terminals. The SCR/Diode arrays do not have a fixed breakover or operating voltage. These devices 'float' between the input and power supply rails and thus the same device can operate at any potential within its range.

Forward Voltage Drop

The maximum forward voltage drop between an input pin and respective power supply pin for a specific forward current.

Reverse Voltage Drop

The maximum reverse voltage drop between an input pin and respective power supply pin for a specific reverse current.

Reverse Standoff Voltage

The device VR should be equal to, or greater than the peak operating level of circuit (or part of the circuit) to be protected. This is to ensure that SPA's do not clip the circuit drive voltage.

Reverse Leakage Current

Maximum of state current measured at specified voltage.

Clamp Voltage

Maximum voltage which can be measured across the protector when subjected to the maximum peak pulse current.

Input Leakage Current

The DC current that is measured at the input pins at the stated voltage supplied to the input.

Quiescent Supply Current

The maximum DC current into V+/V- pins with Vsupply at its maximum voltage

Input Capacitance

The capacitance measured between the input pin and either supply pin at 1MHz/1VRMS applied.

Common Littelfuse SPA Product Applications

Littelfuse SPAs serve a wide range of end product circuit protection applications.

The lists provided here include only a short summary of common SPA applications. For additional information and to discuss your application and requirements in depth, please contact your Littelfuse products representative.

Littelfuse offers extensive application expertise, and validation testing capabilities to help you find the ideal Littelfuse SPA solution to serve your requirements.

Common Cables and Transmission Speeds

Universal Serial Bus (USB) Products:

USB 1.1/2.0 Full Speed (12 Mbp/s)
USB 2.0 Hi-Speed (480 Mbp/s)
USB 3.0 Super-Speed (4.8 Gbp/s -- Coming Soon)

- PCI adapter cards
- Digital cameras
- Peripherals, etc.
- Computers (desktops and laptops)
- Peripherals (printers, scanners, etc.)
- Handheld devices (PDA's, cell phones, MPEG players, etc.)
- Repeaters and hubs
- Digital still cameras

Digital Visual Interface (DVI) Products:

DVI (1.12 Gbp/s)

- Visual Sources
- Desktop and laptop computers
- DVD's and PVR's
- Set top boxes Visual Displays
- LCD and CRT units
- LCD overhead project

IEEE 1394 Products:

IEEE 1394a (400 Mbp/s)
IEEE 1394b (800 to 1,600 Mbp/s -- Coming Soon)

- PCI adapter cards
- Hubs/routers
- Computers (desktops and laptops)
- PCI adapter cards
- Repeaters and hubs
- External hard drives
- Digital video recorders
- Digital still cameras
- Recordable CD ROM drives

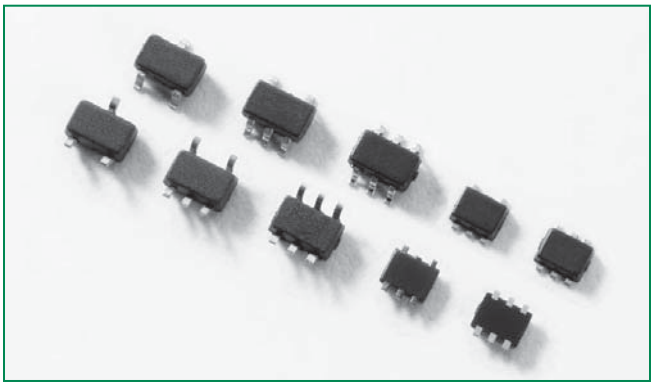
	Littelfuse SPA Series and Product Applications													
	SP1001	SP1002	SP3001	SP3002	SP3003	SP3004	SP050X	SP720	SP721	SP723	SP724	SP725	SP03-6	SPUSB1
Audio Lines														
Cell Phone	X						X	X	X	X	X	X		
LCD TV	X						X	X	X	X	X	X		
Set Top Box	X						X	X	X	X	X	X		
Low speed I/O Ports														
Cell Phone	X						X	X	X	X	X	X		
LCD TV	X						X	X	X	X	X	X		
Set Top Box	X						X	X	X	X	X	X		
USB 1.1 Ports														
Cell Phone	X						X	X	X	X	X	X		X
USB 2.0 Ports														
Cell Phone			X	X	X	X								X
LCD TV			X	X	X	X								X
Set Top Box			X	X	X	X								X
1394 Port														
LCD TV			X	X	X	X								
Set Top Box			X	X	X	X								
HDMI Port														
LCD TV			X	X	X	X								
Set Top Box			X	X	X	X								
LCD Module														
Cell Phone	X		X	X	X	X	X	X	X	X	X	X		
SIM Socket														
Cell Phone	X						X	X	X	X	X	X		
MMC Interface														
Cell Phone	X						X							
Keypads/Buttons														
Cell Phone	X						X	X	X	X	X	X		
Analog Video														
LCD TV		X					X	X	X	X	X	X		
Set Top Box		X					X	X	X	X	X	X		
Ethernet Port														
LCD TV			X	X	X	X							X	
Set Top Box			X	X	X	X							X	

NOTE: The application summaries listed here are for reference only. Determination of suitability for a specific application is the responsibility of the customer.

Suppressors with high capacitance can affect the data stream by distorting the data waveforms. In addition to low-capacitance SPAs, Littelfuse also offers PulseGuard® ESD suppressors as a solution for ESD protection. Both technologies will provide ESD protection and maintain the integrity of the data signals. PulseGuard® ESD products are surface mount devices with 0.050 pF of capacitance.

To assure suitability of any Littelfuse device, be sure to test the device within the end application under conditions of intended use.

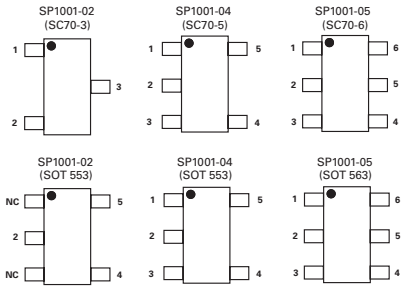
RoHS Pb GREEN SP1001 Lead-Free/Green Series



Description

Zener diodes fabricated in a proprietary silicon avalanche technology protect each I/O pin to provide a high level of protection for electronic equipment that may experience destructive electrostatic discharges (ESD). These robust diodes can safely absorb repetitive ESD strikes at the maximum level specified in the IEC 61000-4-2 international standard (Level 4, 8KV contact discharge) without performance degradation. Their very low loading capacitance also makes them ideal for protecting high-speed signal pins.

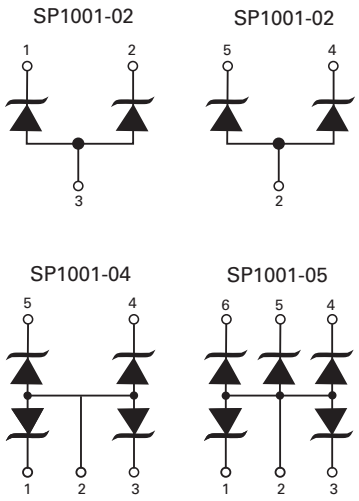
Pinout



Features

- Low capacitance of 8pF (TYP) per I/O
- ESD protection of 8kV contact discharge, 15kV air discharge, (Level 4, IEC61000-4-2)
- EFT protection, IEC61000-4-4, 40A (5/50 ns)
- Low leakage current of 0.5µA (MAX) at 5V
- Small package saves board space

Functional Block Diagram



Applications

- Computer Peripherals
- Mobile Phones
- Digital Cameras
- Desktops/Notebooks
- LCD/PDP TVs
- Set Top Boxes
- DVD Players
- MP3/PMP

Absolute Maximum Ratings

Symbol	Parameter	Value	Units
I_P	Peak Current (t_p=8/20µs)	2	A
T_{OP}	Operating Temperature	-40 to 85	°C
T_{STOR}	Storage Temperature	-60 to 150	°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Thermal Information

Parameter	Rating	Units
Storage Temperature Range	-65 to 150	°C
Maximum Junction Temperature	150	°C
Maximum Lead Temperature (Soldering 10s)	300	°C

Electrical Characteristics (T_{OP} = 25°C)

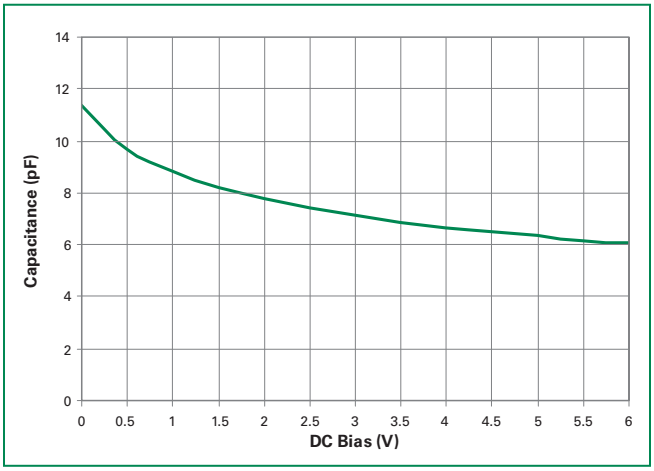
Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Forward Voltage Drop	V_F	I_F=10mA	0.7	0.9	1.2	V
Reverse Voltage Drop	V_R	I_R=10mA	6.0	6.7	8.0	V
Reverse Standoff	V_{RWM}	I_R≤1µA			5.5	V
Reverse Leakage Current	I_{LEAK}	V_R=5V			0.5	µA
Clamp Voltage[1]	V_C	I_{PP}=1A, t_p=8/20µs, Fwd		8.0		V
		I_{PP}=2A, t_p=8/20µs, Fwd		9.6		V
ESD Withstand Voltage[1,2]	V_{ESD}	IEC61000-4-2 (Contact)	±8			kV
		IEC61000-4-2 (Air)	±15			kV
Diode Capacitance[1]	C_D	Reverse Bias=0V		12		pF
		Reverse Bias=2.5V		8		pF
		Reverse Bias=5V		7		pF

Notes:

[1] Parameter is guaranteed by device characterization

[2] A minimum of 1,000 ESD pulses are applied at 1s intervals between the anode and common cathode of each diode

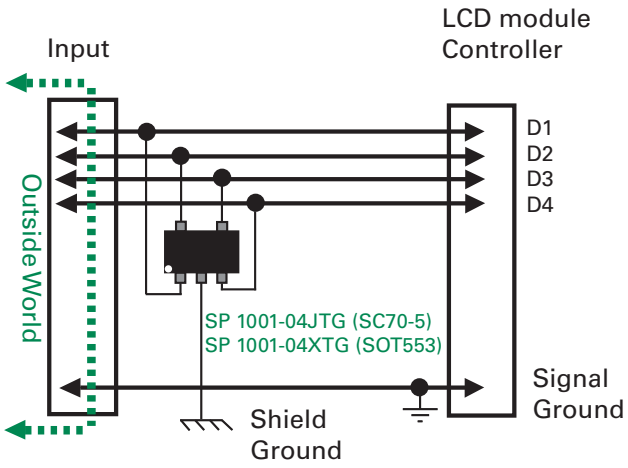
Capacitance vs. Reverse Bias



Design Consideration

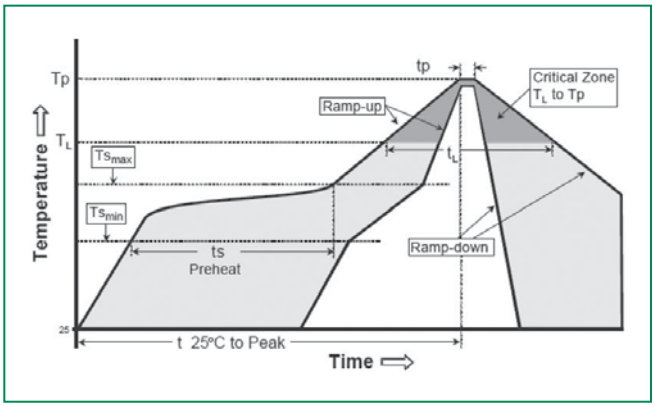
Because of the fast rise-time of the ESD transient, placement of ESD devices is a key design consideration. To achieve optimal ESD suppression, the devices should be placed on the circuit board as close to the source of the ESD transient as possible. Install the ESD suppressors directly behind the connector so that they are the first board-level circuit component encountered by the ESD transient. They are connected from signal/data line to ground.

Application Example



Soldering Parameters

Reflow Condition		Pb – Free assembly
Pre Heat	-Temperature Min ($T_{s(min)}$)	150°C
	-Temperature Max ($T_{s(max)}$)	200°C
	-Time (min to max) (t_s)	60 – 180 secs
Average ramp up rate (Liquidus) Temp (T_L) to peak		3°C/second max
$T_{S(max)}$ to T_L - Ramp-up Rate		3°C/second max
Reflow	-Temperature (T_L) (Liquidus)	217°C
	-Temperature (t_L)	60 – 150 seconds
Peak Temperature (T_P)		$250^{+0/-5}$ °C
Time within 5°C of actual peak Temperature (t_p)		20 – 40 seconds
Ramp-down Rate		6°C/second max
Time 25°C to peak Temperature (T_P)		8 minutes max.
Do not exceed		260°C



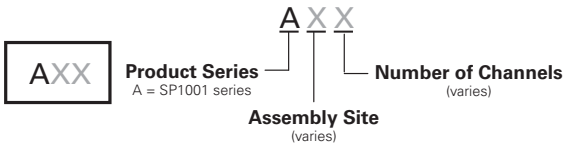
Lead-Free/Green SP1001

Part Numbering System

SP1001-02 J T G

- Silicon Protection Array
- Series
- Number of Channels
  - 02 = 2 Channel
  - 04 = 4 Channel
  - 05 = 5 Channel
- Package
  - J = SC70-3, -5 or -6, 3000 qty
  - X = SOT553 or SOT563, 5000 qty
- T= Tape & Reel
- G= Green

Part Marking System



Product Characteristics

Lead Plating	Matte Tin
Lead Material	Copper Alloy
Lead Coplanarity	0.0004 inches (0.102mm)
Subsitute Material	Silicon
Body Material	Molded Epoxy
Flammability	UL94-V-0

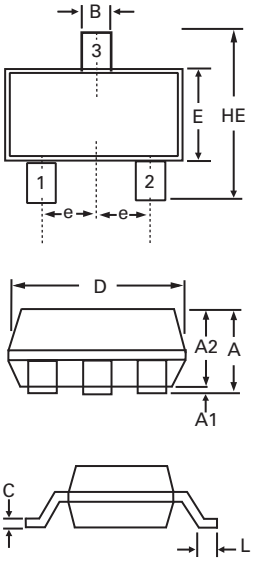
Notes :

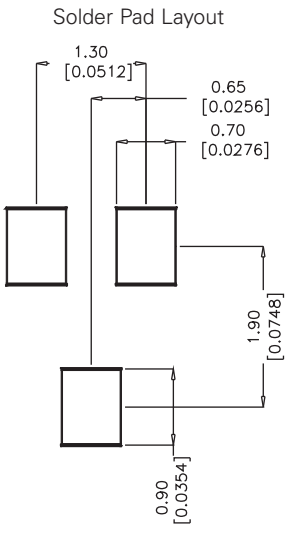
1. All dimensions are in millimeters
2. Dimensions include solder plating.
3. Dimensions are exclusive of mold flash & metal burr.
4. All specifications comply to JEDEC SPEC MO-203 Issue A
5. Blo is facing up for mold and facing down for trim/form, i.e. reverse trim/form.
6. Package surface matte finish VDI 11-13.

Ordering Information

Part Number	Package	Marking	Min. Order Qty.
SP1001-02JTG	SC70-3	AX2	3000
SP1001-02XTG	SOT553	AX2	5000
SP1001-04JTG	SC70-5	AX4	3000
SP1001-04XTG	SOT553	AX4	5000
SP1001-05JTG	SC70-6	AX5	3000
SP1001-05XTG	SOT563	AX5	5000

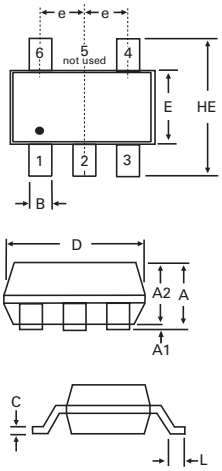
Package Dimensions - SC70-3



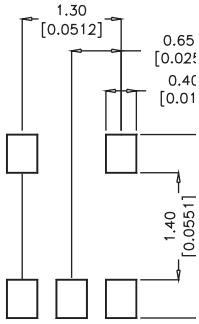


Package	SC70-3			
Pins	3			
JEDEC	MO-203 Issue A			
	Millimeters		Inches	
	Min	Max	Min	Max
A	0.80	1.10	0.031	0.043
A1	0.00	0.10	0.000	0.004
A2	0.70	1.00	0.028	0.039
B	0.15	0.30	0.006	0.012
c	0.08	0.25	0.003	0.010
D	1.85	2.25	0.073	0.089
E	1.15	1.35	0.045	0.053
e	0.66 BSC		0.026 BSC	
HE	2.00	2.40	0.079	0.094
L	0.26	0.46	0.010	0.018

Package Dimensions - SC70-5

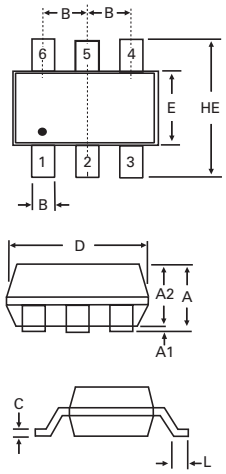


Solder Pad Layout

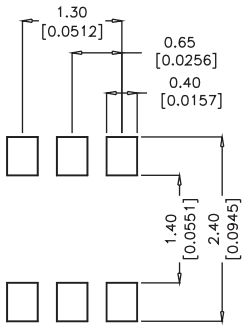


Package	SC70-5			
Pins	5			
JEDEC	MO-203 Issue A			
	Millimeters		Inches	
	Min	Max	Min	Max
A	0.80	1.10	0.031	0.043
A1	0.00	0.10	0.000	0.004
A2	0.70	1.00	0.028	0.039
B	0.15	0.30	0.006	0.012
c	0.08	0.25	0.003	0.010
D	1.85	2.25	0.073	0.089
E	1.15	1.35	0.045	0.053
e	0.65 BSC		0.026 BSC	
HE	2.00	2.40	0.079	0.094
L	0.26	0.46	0.010	0.018

Package Dimensions - SC70-6

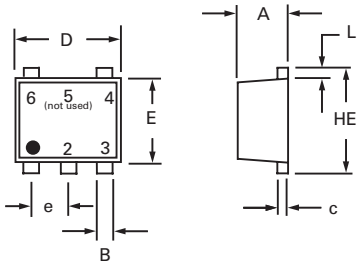


Solder Pad Layout

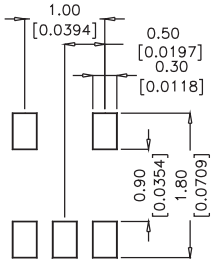


Package	SC70-6			
Pins	6			
JEDEC	MO-203 Issue A			
	Millimeters		Inches	
	Min	Max	Min	Max
A	0.80	1.10	0.031	0.043
A1	0.00	0.10	0.000	0.004
A2	0.70	1.00	0.028	0.039
B	0.15	0.30	0.006	0.012
c	0.08	0.25	0.003	0.010
D	1.85	2.25	0.073	0.089
E	1.15	1.35	0.045	0.053
e	0.65 BSC		0.026 BSC	
HE	2.00	2.40	0.079	0.094
L	0.26	0.46	0.010	0.018

Package Dimensions - SOT553

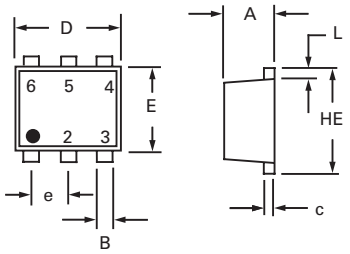


Solder Pad Layout

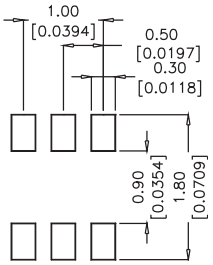


Package	SOT 553			
Pins	5			
	Millimeters		Inches	
	Min	Max	Min	Max
A	0.50	0.60	0.020	0.024
B	0.17	0.27	0.007	0.011
c	0.08	0.018	0.003	0.007
D	1.50	1.70	0.059	0.067
E	1.10	1.30	0.043	0.051
e	0.50 BSC		0.014 BSC	
L	0.10	0.30	0.004	0.012
HE	1.50	1.70	0.059	0.067

Package Dimensions - SOT563

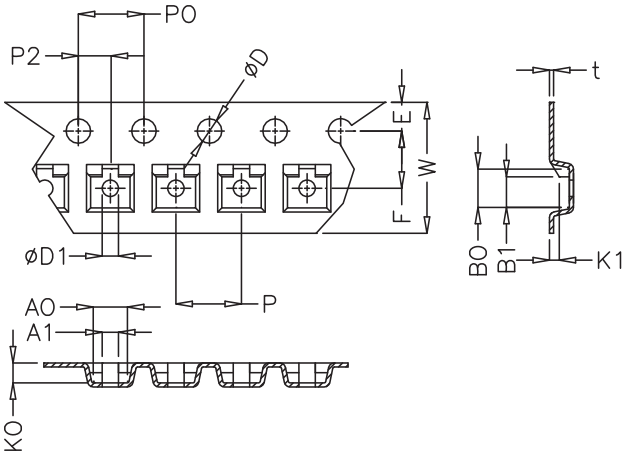


Solder Pad Layout



Package	SOT 563			
Pins	6			
	Millimeters		Inches	
	Min	Max	Min	Max
A	0.50	0.60	0.020	0.024
B	0.17	0.27	0.007	0.011
c	0.08	0.18	0.003	0.007
D	1.50	1.70	0.059	0.067
E	1.10	1.30	0.043	0.051
e	0.50 BSC		0.020 BSC	
L	0.10	0.30	0.004	0.012
HE	1.50	1.70	0.059	0.067

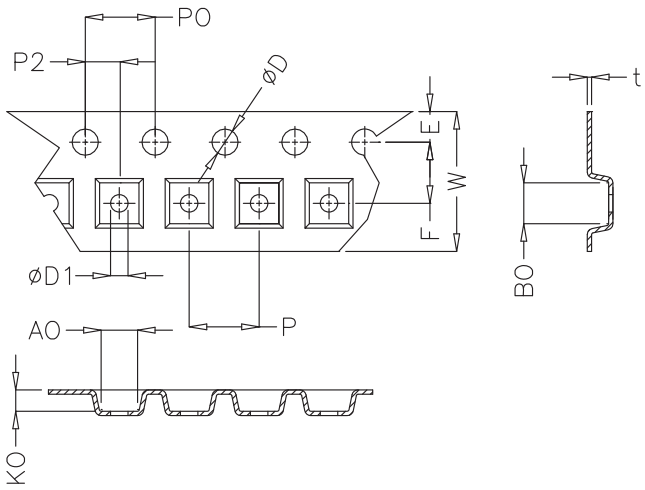
Embossed Carrier Tape & Reel Specification - SC70-3



Dimensions

	Millimetres		Inches	
	Min	Max	Min	Max
E	1.65	1.85	0.065	0.073
F	3.45	3.55	0.135	0.139
P2	1.95	2.05	0.077	0.081
D	1.40	1.60	0.055	0.063
D1	1.00	1.25	0.039	0.049
P0	3.90	4.10	0.154	0.161
10P0	40.0 +/- 0.20		1.574 +/- 0.008	
W	7.70	8.10	0.303	0.318
P	3.90	4.10	0.153	0.161
A0	2.30	2.50	0.090	0.098
A1	1.00 Ref		0.039 Ref	
B0	2.30	2.50	0.090	0.098
B1	1.90 Ref		0.074	
K0	1.10	1.30	0.043	0.051
K1	0.60 Ref		0.023 Ref	
t	0.27 max		0.010	

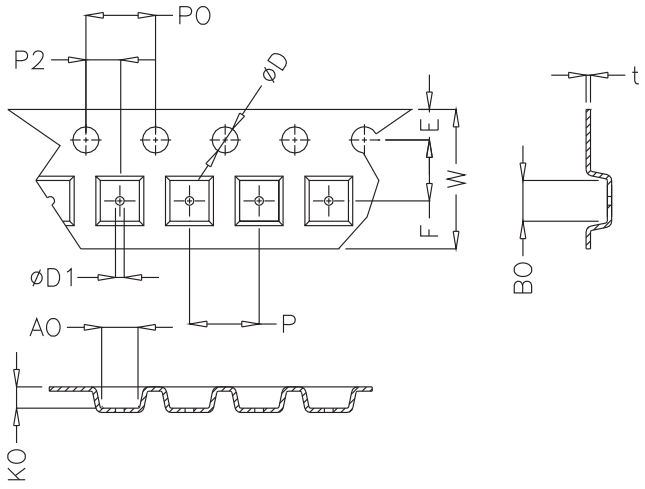
Embossed Carrier Tape & Reel Specification - SC70-5 and SC70-6



Dimensions

	Millimetres		Inches	
	Min	Max	Min	Max
E	1.65	1.85	0.065	0.073
F	3.45	3.55	0.135	0.139
P2	1.95	2.05	0.077	0.081
D	1.40	1.60	0.055	0.063
D1	1.00	1.25	0.039	0.049
P0	3.90	4.10	0.154	0.161
10P0	40.0 +/- 0.20		1.574 +/- 0.008	
W	7.70	8.10	0.303	0.318
P	3.90	4.10	0.153	0.161
A0	2.14	2.34	0.084	0.092
B0	2.24	2.44	0.088	0.096
K0	1.12	1.32	0.044	0.051
t	0.27 max		0.010 max	

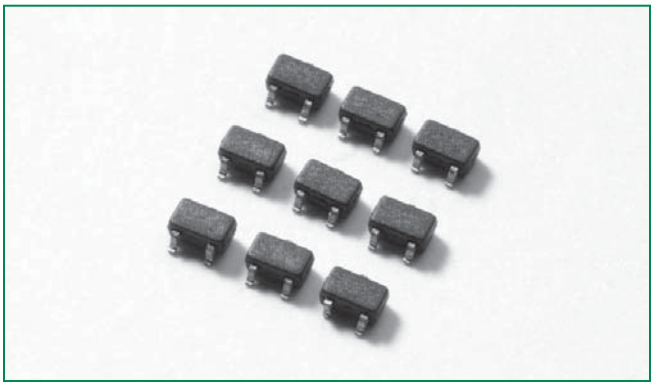
Embossed Carrier Tape & Reel Specification - SOT553 and SOT563



Dimensions

	Millimetres		Inches	
	Min	Max	Min	Max
E	1.65	1.85	0.065	0.073
F	3.45	3.55	0.135	0.139
P2	1.95	2.05	0.077	0.081
D	1.40	1.60	0.055	0.063
D1	0.45	0.55	0.017	0.021
P0	3.90	4.1	0.154	0.161
10P0	40.0 +/- 0.20		1.574 +/- 0.008	
W	7.70	8.10	0.303	0.318
P	3.90	4.10	0.153	0.161
A0	1.73	1.83	0.068	0.072
B0	1.73	1.83	0.068	0.072
K0	0.64	0.74	0.025	0.029
t	0.22 max		0.010 max	

RoHS Pb GREEN SP1002 Lead-Free/Green Series

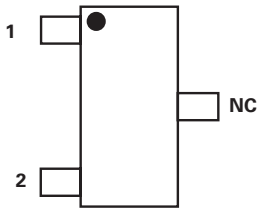


Description

Back-to-Back Zener diodes fabricated in a proprietary silicon avalanche technology protect each I/O pin to provide a high level of protection for electronic equipment that may experience destructive electrostatic discharges (ESD). These robust diodes can safely absorb repetitive ESD strikes at the maximum level specified in the IEC 61000-4-2 international standard (Level 4, 8KV contact discharge) without performance degradation. Their very low loading capacitance also makes them ideal for protecting high-speed signal pins.

Pinout

SP1002-01
(SC70-3)



Features

- Low capacitance of 5pF (TYP) I/O to I/O
- ESD protection of 8kV contact discharge, 15kV air discharge, (Level 4, IEC61000-4-2)
- EFT protection, IEC61000-4-4, 40A (5/50 ns)
- Low leakage current of 0.5µA (MAX) at 5V
- Small package saves board space

Functional Block Diagram

SP1002-01

Applications

- Computer Peripherals
- Mobile Phones
- Digital Cameras
- Desktops/Notebooks
- LCD/PDP TVs
- Set Top Boxes
- DVD Players
- MP3/PMP

Absolute Maximum Ratings

Symbol	Parameter	Value	Units
I_P	Peak Current (t_p=8/20µs)	2	A
T_{OP}	Operating Temperature	-40 to 85	°C
T_{STOR}	Storage Temperature	-60 to 150	°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Thermal Information

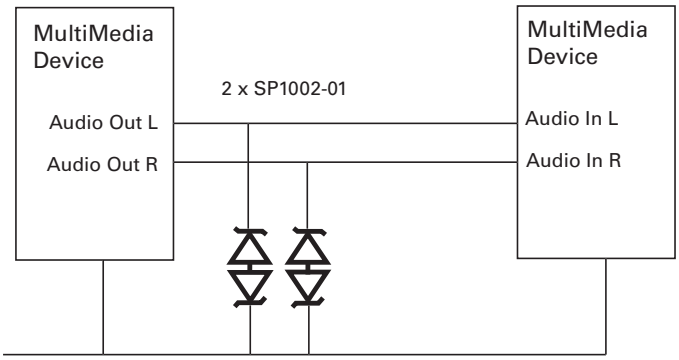
Parameter	Rating	Units
Storage Temperature Range	-65 to 150	°C
Maximum Junction Temperature	150	°C
Maximum Lead Temperature (Soldering 10s)	300	°C

Electrical Characteristics (T_{OP} = 25°C)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Voltage Drop	V_D	I_R=10mA	6.0	7.0	8.5	V
Standoff Voltage	V_{RWM}	I_R≤1µA with 1 I/O at GND			6.0	V
Leakage Current	I_{LEAK}	V_R=5V with I/O at GND			0.5	µA
Clamp Voltage[1]	V_C	I_{PP}=1A, t_p=8/20µs, Fwd		9.2		V
		I_{PP}=2A, t_p=8/20µs, Fwd		11.2		V
ESD Withstand Voltage[1,3]	V_{ESD}	IEC61000-4-2 (Contact)	±8			kV
		IEC61000-4-2 (Air)	±15			kV
Diode Capacitance[1]	C_D	Reverse Bias=0V		6		pF
		Reverse Bias=2.5V		5		pF
		Reverse Bias=5V		5		pF

Notes:
[1] Parameter is guaranteed by device characterization
[2] A minimum of 1,000 ESD pulses are applied at 1s intervals

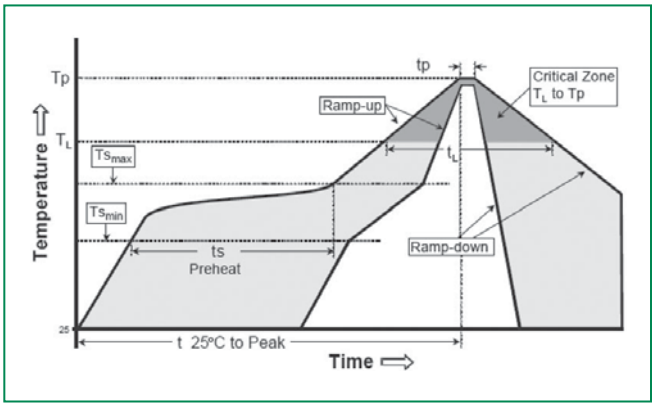
Application Example



SCART MultiMedia Application of SP1002-01

Soldering Parameters

Reflow Condition		Pb – Free assembly
Pre Heat	-Temperature Min ($T_{s(min)}$)	150°C
	-Temperature Max ($T_{s(max)}$)	200°C
	-Time (min to max) (t_s)	60 – 180 secs
Average ramp up rate (Liquidus) Temp (T_L) to peak		3°C/second max
$T_{S(max)}$ to T_L - Ramp-up Rate		3°C/second max
Reflow	-Temperature (T_L) (Liquidus)	217°C
	-Temperature (t_L)	60 – 150 seconds
Peak Temperature (T_P)		$250^{+0/-5}$ °C
Time within 5°C of actual peak Temperature (t_p)		20 – 40 seconds
Ramp-down Rate		6°C/second max
Time 25°C to peak Temperature (T_P)		8 minutes max.
Do not exceed		260°C



Part Numbering System

SP1002-01JTG

- Silicon Protection Array
- Series
- Number of Channels
- Package
  - J = SC70-3, 3000 qty
- T= Tape & Reel
- G= Green

Part Marking System

BX1

- **Product Series**
  - A = SP1002 series
- **Assembly Site**
  - (varies)
- **Number of Channels**

Product Characteristics

Lead Plating	Matte Tin
Lead Material	Copper Alloy
Lead Coplanarity	0.0004 inches (0.102mm)
Subsitute Material	Silicon
Body Material	Molded Epoxy
Flammability	UL94-V-0

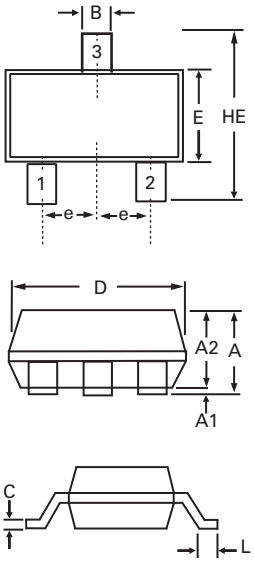
Notes :

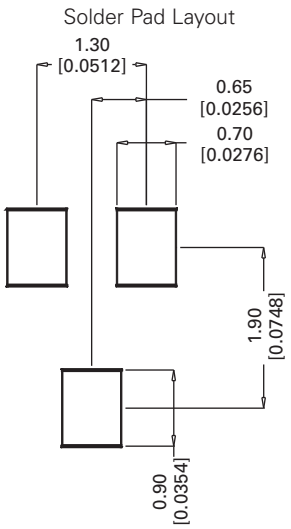
1. All dimensions are in millimeters
2. Dimensions include solder plating.
3. Dimensions are exclusive of mold flash & metal burr.
4. All specifications comply to JEDEC SPEC MO-203 Issue A
5. Blo is facing up for mold and facing down for trim/form, i.e. reverse trim/form.
6. Package surface matte finish VDI 11-13.

Ordering Information

Part Number	Package	Marking	Min. Order Qty.
SP1002-01JTG	SC70-3	BX1	3000

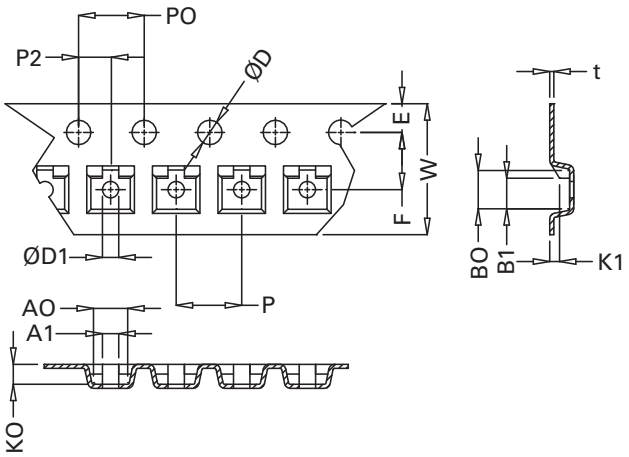
Package Dimensions - SC70-3





Package	SC70-3			
Pins	3			
JEDEC	MO-203 Issue A			
	Millimeters		Inches	
	Min	Max	Min	Max
A	0.80	1.10	0.031	0.043
A1	0.00	0.10	0.000	0.004
A2	0.70	1.00	0.028	0.039
B	0.15	0.30	0.006	0.012
c	0.08	0.25	0.003	0.010
D	1.85	2.25	0.073	0.089
E	1.15	1.35	0.045	0.053
e	0.66 BSC		0.026 BSC	
HE	2.00	2.40	0.079	0.094
L	0.26	0.46	0.010	0.018

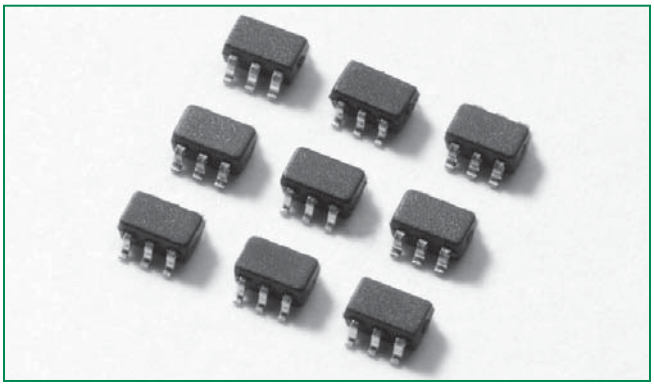
Embossed Carrier Tape & Reel Specification - SC70-3



Dimensions

	Millimetres		Inches	
	Min	Max	Min	Max
E	1.65	1.85	0.065	0.073
F	3.45	3.55	0.135	0.139
P2	1.95	2.05	0.077	0.081
D	1.40	1.60	0.055	0.063
D1	1.00	1.25	0.039	0.049
P0	3.90	4.10	0.154	0.161
10P0	40.0 +/- 0.20		1.574 +/- 0.008	
W	7.70	8.10	0.303	0.318
P	3.90	4.10	0.153	0.161
A0	2.30	2.50	0.090	0.098
A1	1.00 Ref		0.039 Ref	
B0	2.30	2.50	0.090	0.098
B1	1.90 Ref		0.074	
K0	1.10	1.30	0.043	0.051
K1	0.60 Ref		0.023 Ref	
t	0.27 max		0.010	

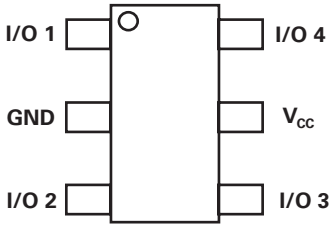
RoHS Pb GREEN SP3001 Lead-Free/Green Series



Description

The SP3001 has ultra low capacitance rail-to rail diodes with an additional zener diode fabricated in a proprietary silicon avalanche technology to protect each I/O pin providing a high level of protection for electronic equipment that may experience destructive electrostatic discharges (ESD). These robust diodes can safely absorb repetitive ESD strikes at the maximum level specified in the IEC 61000-4-2 international standard (Level 4, 8KV contact discharge) without performance degradation. Their very low loading capacitance also makes them ideal for protecting high speed signal pins such as HDMI, DVI, USB2.0, and IEEE 1394.

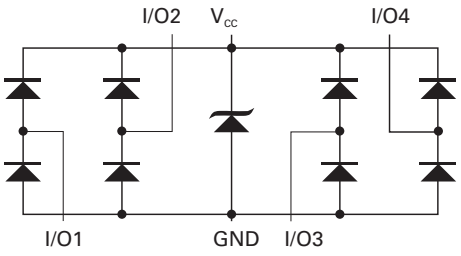
Pinout



Features

- Low capacitance of 0.65pF (TYP) per I/O
- ESD protection of ±8kV contact discharge, ±15kV air discharge, (IEC61000-4-2)
- EFT protection, IEC61000-4-4, 40A (5/50 ns)
- Low leakage current of 0.5µA (MAX) at 5V
- Small SC70 package saves board space

Functional Block Diagram



Applications

- Computer Peripherals
- Mobile Phones
- PDA's
- Digital Cameras
- Network Hardware/Ports
- Test Equipment
- Medical Equipment

Absolute Maximum Ratings

Symbol	Parameter	Value	Units
I_P	Peak Current (t_p=8/20µs)	2.5	A
T_{OP}	Operating Temperature	-40 to 85	°C
T_{STOR}	Storage Temperature	-50 to 150	°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Thermal Information

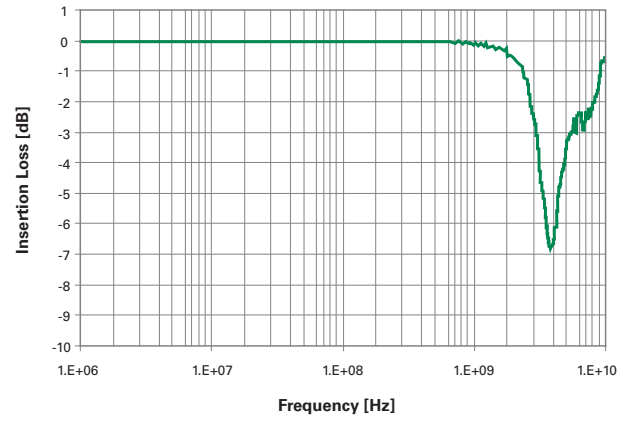
Parameter	Rating	Units
Storage Temperature Range	-65 to 150	°C
Maximum Junction Temperature	150	°C
Maximum Lead Temperature (Soldering 10s)	300	°C

Electrical Characteristics (T_{OP}=25°C)

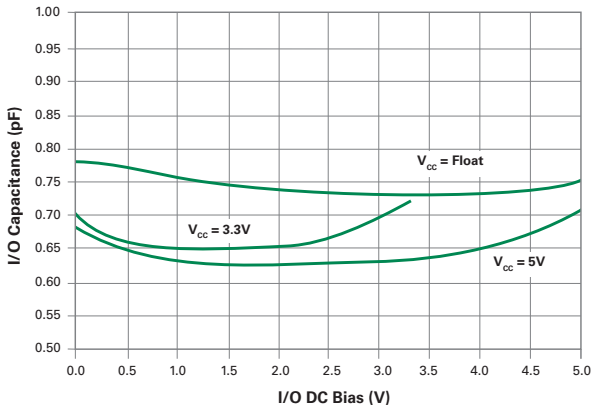
Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Zener Breakdown Voltage	V_{BR}	I_R=10µA	6.0			V
Reverse Leakage Current	I_{LEAK}	V_R=5V			0.5	µA
Clamp Voltage[1]	V_C	I_{PP}=1A, t_p=8/20µs, Fwd		9.5		V
		I_{PP}=2A, t_p=8/20µs, Fwd		10.6		V
ESD Withstand Voltage[1]	V_{ESD}	IEC61000-4-2 (Contact)	±8			kV
		IEC61000-4-2 (Air)	±15			kV
Diode Capacitance[1]	$C_{I/O-GND}$	Reverse Bias=0V		0.80		pF
		Reverse Bias=1.65V		0.65		pF
Diode Capacitance[1]	$C_{I/O-I/O}$	Reverse Bias=0V		0.35		pF

Note 1: Parameter is guaranteed by device characterization

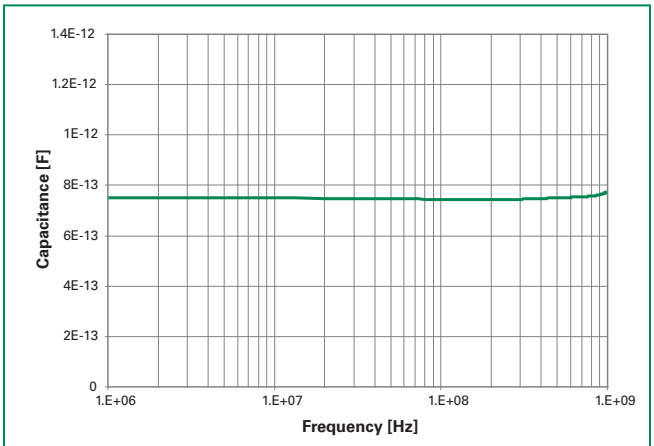
Insertion Loss (S21) I/O to GND



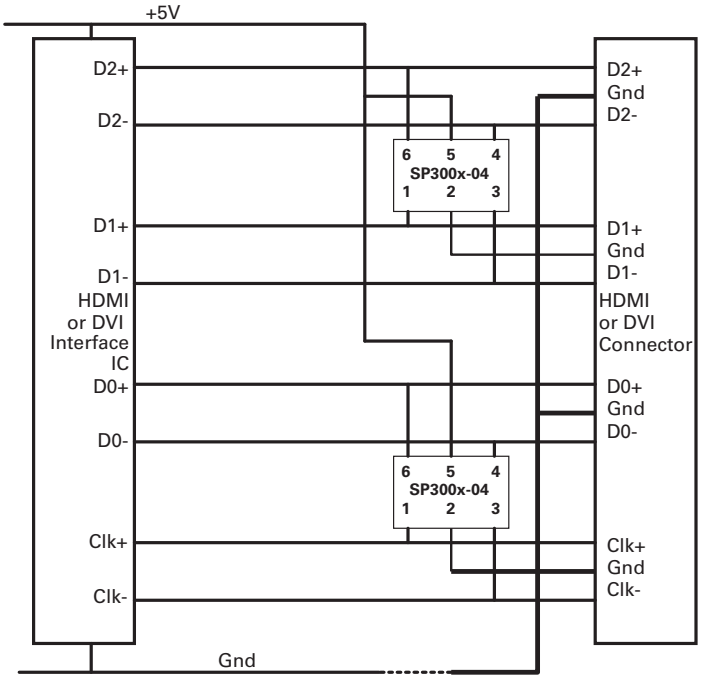
Capacitance vs. Bias Voltage



Capacitance vs. Frequency



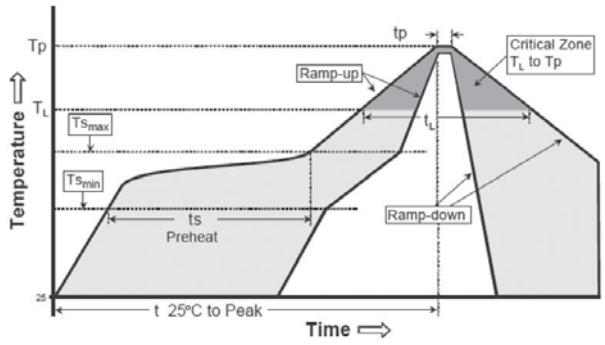
Application Example



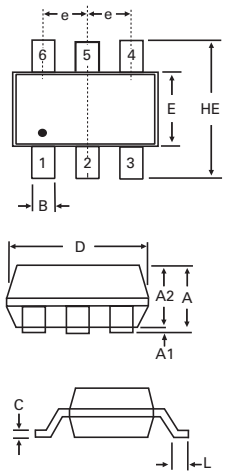
HDMI or DVI application example for the Littelfuse SP300x-04 protection devices. A single 4 channel SP300x-04 device can be used to protect four of the data lines in a HDMI/DVI interface. Two (2) SP300x-04 devices provide protection for the main data lines. Low voltage ASIC HDMI/DVI drivers can also be protected with the SP300x-04, the $+V_{CC}$ pins on the SP300x-04 can be substituted with a suitable bypass capacitor or in some backdrive applications the $+V_{CC}$ of the SP300x-04 can be floated or NC.

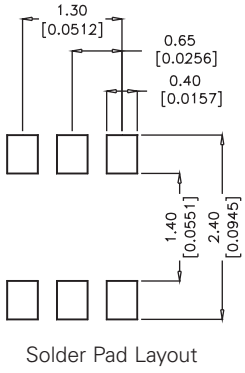
Soldering Parameters

Reflow Condition		Pb – Free assembly
Pre Heat	-Temperature Min ($T_{s(min)}$)	150°C
	-Temperature Max ($T_{s(max)}$)	200°C
	-Time (min to max) (t_s)	60 – 180 secs
Average ramp up rate (Liquidus) Temp (T_L) to peak		3°C/second max
$T_{S(max)}$ to T_L - Ramp-up Rate		3°C/second max
Reflow	-Temperature (T_L) (Liquidus)	217°C
	-Temperature (t_L)	60 – 150 seconds
Peak Temperature (T_P)		$250^{+0/-5}$ °C
Time within 5°C of actual peak Temperature (t_P)		20 – 40 seconds
Ramp-down Rate		6°C/second max
Time 25°C to peak Temperature (T_P)		8 minutes Max.
Do not exceed		260°C



Package Dimensions - SC70-6





Solder Pad Layout

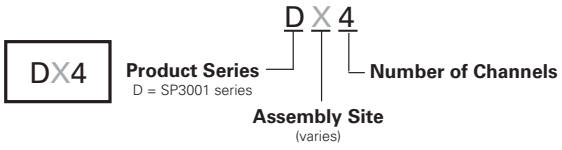
Package	SC70-6			
Pins	6			
JEDEC	MO-203 Issue A			
	Millimeters		Inches	
	Min	Max	Min	Max
A	0.80	1.10	0.031	0.043
A1	0.00	0.10	0.000	0.004
A2	0.70	1.00	0.028	0.039
B	0.15	0.30	0.006	0.012
c	0.08	0.25	0.003	0.010
D	1.85	2.25	0.073	0.089
E	1.15	1.35	0.045	0.053
e	0.65 BSC		0.026 BSC	
HE	2.00	2.40	0.079	0.094
L	0.26	0.46	0.010	0.018

Part Numbering System

SP3001-04JTG

- Silicon Protection Array
- Series
- Number of Channels
  -04 = 4 channel
- Package
  J = SC70-6, 3000 quantity
- T= Tape & Reel
- G= Green

Part Marking System



Product Characteristics

Lead Plating	Matte Tin
Lead Material	Copper Alloy
Lead Coplanarity	0.0004 inches (0.102mm)
Subsitute Material	Silicon
Body Material	Molded Epoxy
Flammability	UL94-V-0

Notes :

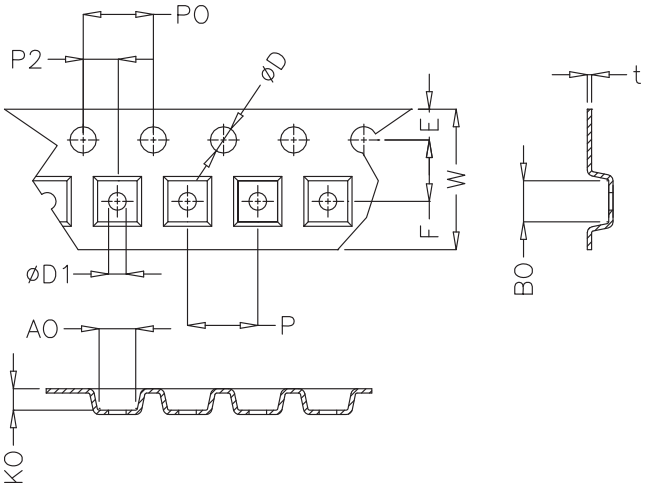
1. All dimensions are in millimeters
2. Dimensions include solder plating.
3. Dimensions are exclusive of mold flash & metal burr.
4. All specifications comply to JEDEC SPEC MO-223 Issue A
5. Blo is facing up for mold and facing down for trim/form, i.e. reverse trim/form.
6. Package surface matte finish VDI 11-13.

Ordering Information

Part Number	Package	Marking	Min. Order Qty.
SP3001-04JTG	SC70-6	DX4	3000

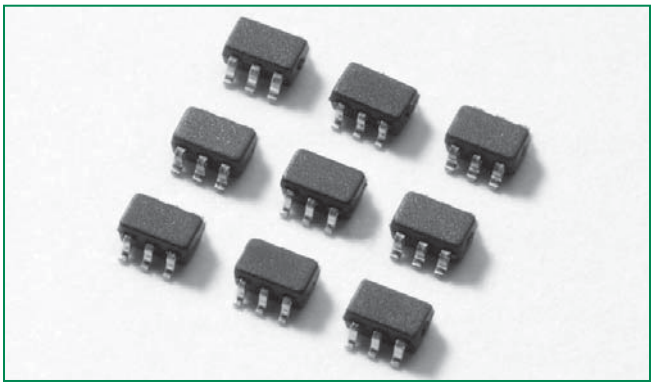
Lead-Free/Green SP3001

Embossed Carrier Tape & Reel Specification - SC70-6



Symbol	Millimetres		Inches	
	Min	Max	Min	Max
E	1.65	1.85	0.064	0.072
F	3.45	3.55	0.135	0.139
P2	1.95	2.05	0.076	0.080
D	1.40	1.60	0.055	0.062
D1	1.00	1.25	0.039	0.049
P0	3.90	4.10	0.153	0.161
10P0	40.0+/- 0.20		1.574+/-0.007	
W	7.70	8.10	0.303	0.318
P	3.90	4.10	0.153	0.161
A0	2.14	2.34	0.084	0.092
B0	2.24	2.44	0.088	0.960
K0	1.12	1.32	0.044	0.052
t	0.27 max		0.010 max	

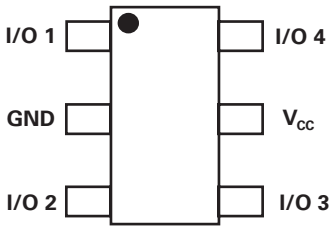
RoHS Pb GREEN SP3002 Lead-Free/Green Series



Description

The SP3002 has ultra low capacitance rail-to rail diodes with an additional zener diode fabricated in a proprietary silicon avalanche technology to protect each I/O pin providing a high level of protection for electronic equipment that may experience destructive electrostatic discharges (ESD). These robust diodes can safely absorb repetitive ESD strikes at the maximum level (Level 4) specified in the IEC 61000-4-2 international standard without performance degradation. Their very low loading capacitance also makes them ideal for protecting high speed signal pins such as HDMI, DVI, USB2.0, and IEEE 1394.

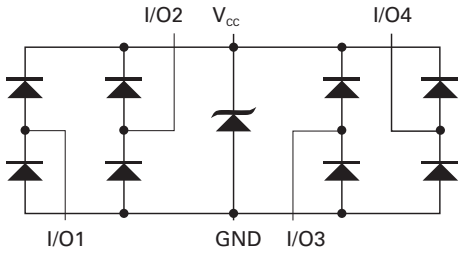
Pinout



Features

- Low capacitance of 0.85 pF (TYP) per I/O
- ESD protection of ±12kV contact discharge, ±15kV air discharge, (IEC61000-4-2)
- EFT protection, IEC61000-4-4, 40A (5/50 ns)
- Low leakage current of 0.5µA (MAX) at 5V
- Small SC70 package saves board space

Functional Block Diagram



Applications

- Computer Peripherals
- Mobile Phones
- PDA's
- Digital Cameras
- Network Hardware/Ports
- Test Equipment
- Medical Equipment

Absolute Maximum Ratings

Symbol	Parameter	Value	Units
I_P	Peak Current (t_p=8/20µs)	4.5	A
T_{OP}	Operating Temperature	-40 to 85	°C
T_{STOR}	Storage Temperature	-50 to 150	°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Thermal Information

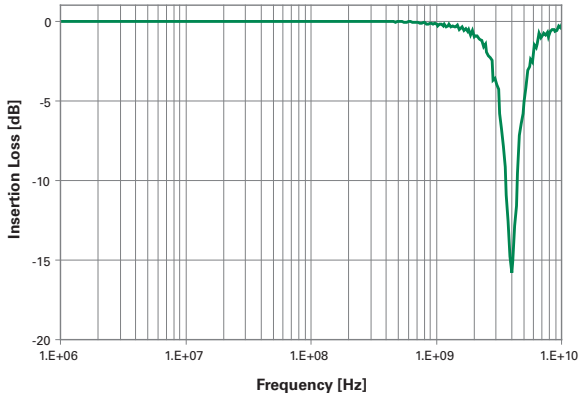
Parameter	Rating	Units
Storage Temperature Range	-65 to 150	°C
Maximum Junction Temperature	150	°C
Maximum Lead Temperature (Soldering 10s)	300	°C

Electrical Characteristics (T_{OP}=25°C)

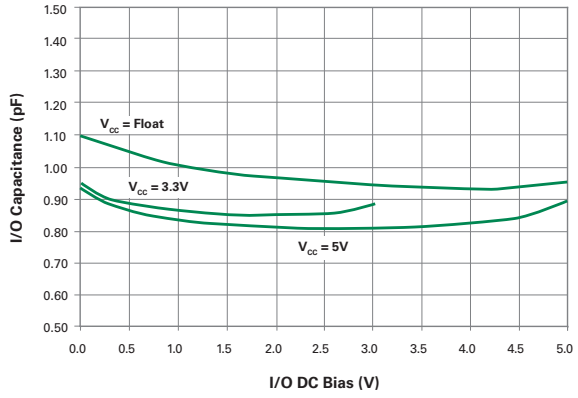
Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Zener Breakdown Voltage	V_{BR}	I_R=10µA	6.0			V
Reverse Leakage Current	I_{LEAK}	V_R=5V			0.5	µA
Clamp Voltage[1]	V_C	I_{PP}=1A, t_p=8/20µs, Fwd		9.5		V
		I_{PP}=2A, t_p=8/20µs, Fwd		10.6		V
ESD Withstand Voltage[1]	V_{ESD}	IEC61000-4-2 (Contact)	±12			kV
		IEC61000-4-2 (Air)	±15			kV
Diode Capacitance[1]	$C_{I/O-GND}$	Reverse Bias=0V		1.1		pF
		Reverse Bias=1.65V		0.85		pF
Diode Capacitance[1]	$C_{I/O-I/O}$	Reverse Bias=0V		0.5		pF

Note 1: Parameter is guaranteed by device characterization

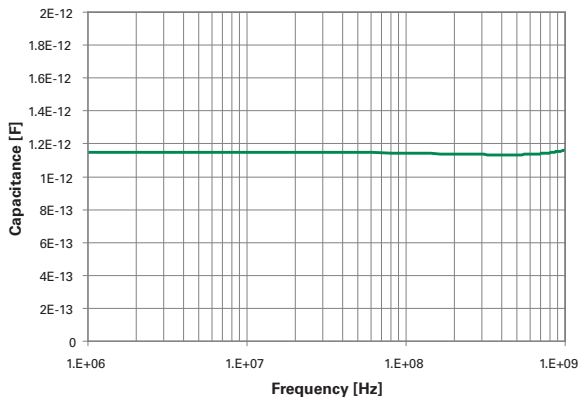
Insertion Loss (S21) I/O to GND



Capacitance vs. Bias Voltage

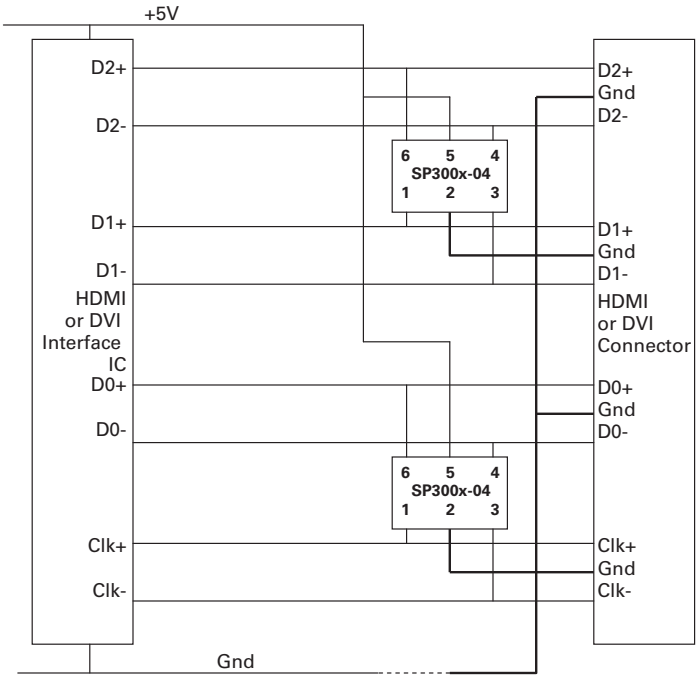


Capacitance vs. Frequency



Lead-Free/Green SP3002

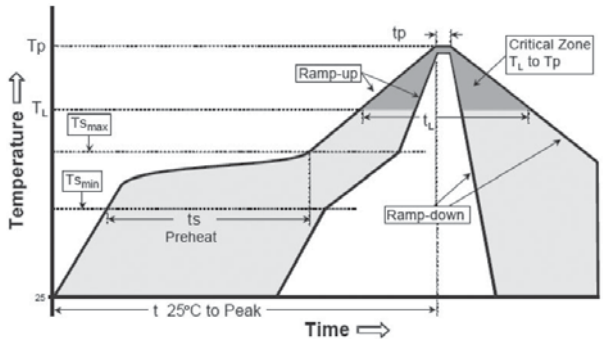
Application Example



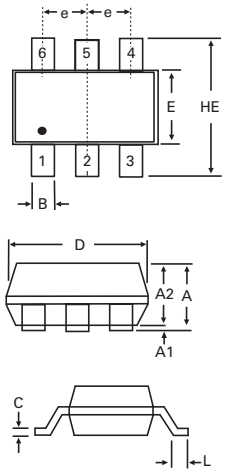
HDMI or DVI application example for the Littelfuse SP300x-04 protection devices. A single 4 channel SP300x-04 device can be used to protect four of the data lines in a HDMI/DVI interface. Two (2) SP300x-04 devices provide protection for the main data lines. Low voltage ASIC HDMI/DVI drivers can also be protected with the SP300x-04, the $+V_{CC}$ pins on the SP300x-04 can be substituted with a suitable bypass capacitor or in some backdrive applications the $+V_{CC}$ of the SP300x-04 can be floated or NC.

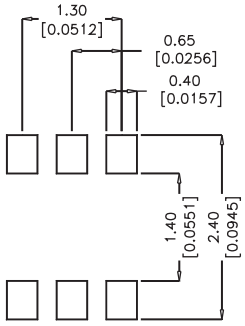
Soldering Parameters

Reflow Condition		Pb – Free assembly
Pre Heat	-Temperature Min ($T_{s(min)}$)	150°C
	-Temperature Max ($T_{s(max)}$)	200°C
	-Time (min to max) (t_s)	60 – 180 secs
Average ramp up rate (Liquidus) Temp (T_L) to peak		3°C/second max
$T_{S(max)}$ to T_L - Ramp-up Rate		3°C/second max
Reflow	-Temperature (T_L) (Liquidus)	217°C
	-Temperature (t_L)	60 – 150 seconds
Peak Temperature (T_P)		$250^{+0/-5}$ °C
Time within 5°C of actual peak Temperature (t_p)		20 – 40 seconds
Ramp-down Rate		6°C/second max
Time 25°C to peak Temperature (T_P)		8 minutes Max.
Do not exceed		260°C



Package Dimensions - SC70-6





Solder Pad Layout

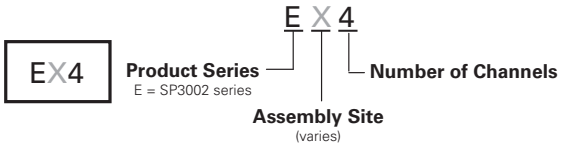
Package	SC70-6			
Pins	6			
JEDEC	MO-203 Issue A			
	Millimeters		Inches	
	Min	Max	Min	Max
A	0.80	1.10	0.031	0.043
A1	0.00	0.10	0.000	0.004
A2	0.70	1.00	0.028	0.039
B	0.15	0.30	0.006	0.012
c	0.08	0.25	0.003	0.010
D	1.85	2.25	0.073	0.089
E	1.15	1.35	0.045	0.053
e	0.65 BSC		0.026 BSC	
HE	2.00	2.40	0.079	0.094
L	0.26	0.46	0.010	0.018

Part Numbering System

SP3002-04JTG

- Silicon Protection Array
- Series
- Number of Channels
  -04 = 4 channel
- Package
  J = SC70-6, 3000 quantity
- T= Tape & Reel
- G= Green

Part Marking System



Product Characteristics

Lead Plating	Matte Tin
Lead Material	Copper Alloy
Lead Coplanarity	0.0004 inches (0.102mm)
Subsitute Material	Silicon
Body Material	Molded Epoxy
Flammability	UL94-V-0

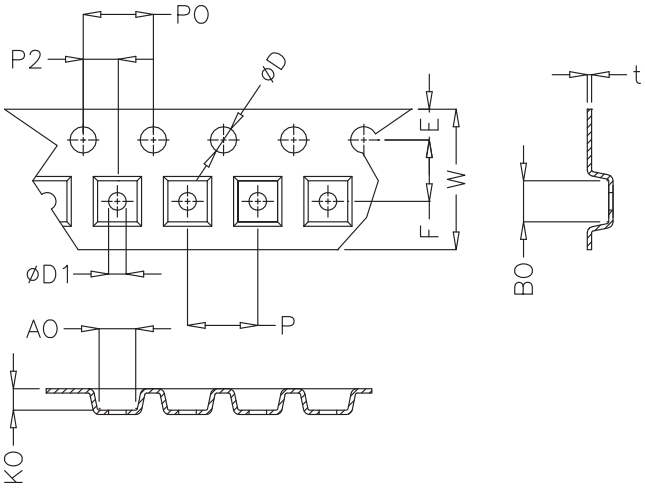
Notes :

1. All dimensions are in millimeters
2. Dimensions include solder plating.
3. Dimensions are exclusive of mold flash & metal burr.
4. All specifications comply to JEDEC SPEC MO-223 Issue A
5. Blo is facing up for mold and facing down for trim/form, i.e. reverse trim/form.
6. Package surface matte finish VDI 11-13.

Ordering Information

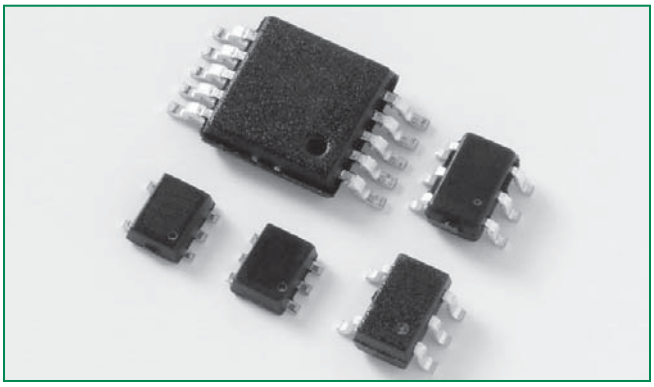
Part Number	Package	Marking	Min. Order Qty.
SP3002-04JTG	SC70-6	EX4	3000

Embossed Carrier Tape & Reel Specification - SC70-6



Symbol	Millimetres		Inches	
	Min	Max	Min	Max
E	1.65	1.85	0.064	0.072
F	3.45	3.55	0.135	0.139
P2	1.95	2.05	0.076	0.080
D	1.40	1.60	0.055	0.062
D1	1.00	1.25	0.039	0.049
P0	3.90	4.10	0.153	0.161
10P0	40.0+/- 0.20		1.574+/-0.007	
W	7.70	8.10	0.303	0.318
P	3.90	4.10	0.153	0.161
A0	2.14	2.34	0.084	0.092
B0	2.24	2.44	0.088	0.960
K0	1.12	1.32	0.044	0.052
t	0.27 max		0.010 max	

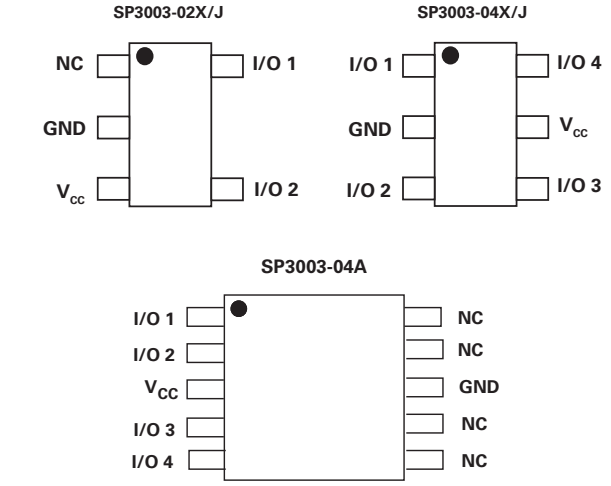
RoHS Pb GREEN SP3003 Lead-Free/Green Series



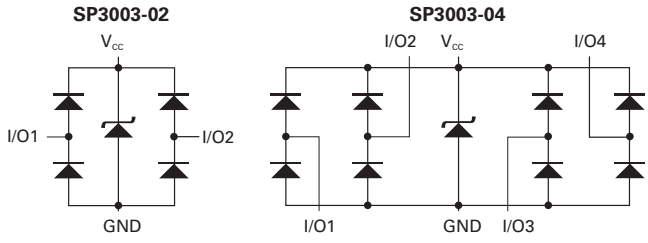
Description

The SP3003 has ultra low capacitance rail-to rail diodes with an additional zener diode fabricated in a proprietary silicon avalanche technology to protect each I/O pin providing a high level of protection for electronic equipment that may experience destructive electrostatic discharges (ESD). These robust diodes can safely absorb repetitive ESD strikes at the maximum level specified in the IEC 61000-4-2 international standard (Level 4, 8KV contact discharge) without performance degradation. Their very low loading capacitance also makes them ideal for protecting high speed signal pins such as HDMI, DVI, USB2.0, and IEEE 1394.

Pinout



Functional Block Diagram



Features

- Low capacitance of 0.65pF (TYP) per I/O
- ESD protection of ±8kV contact discharge, ±15kV air discharge, (IEC61000-4-2)
- EFT protection, IEC61000-4-4, 40A (5/50 ns)
- Low leakage current of 0.5µA (MAX) at 5V
- Small packages save board space (SC70, SOT553, SOT563, MSOP10)

Applications

- Computer Peripherals
- Mobile Phones
- PDA's
- Digital Cameras
- Network Hardware/Ports
- Test Equipment
- Medical Equipment

Absolute Maximum Ratings

Symbol	Parameter	Value	Units
I_P	Peak Current (t_p=8/20µs)	2.5	A
T_{OP}	Operating Temperature	-40 to 85	°C
T_{STOR}	Storage Temperature	-50 to 150	°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Thermal Information

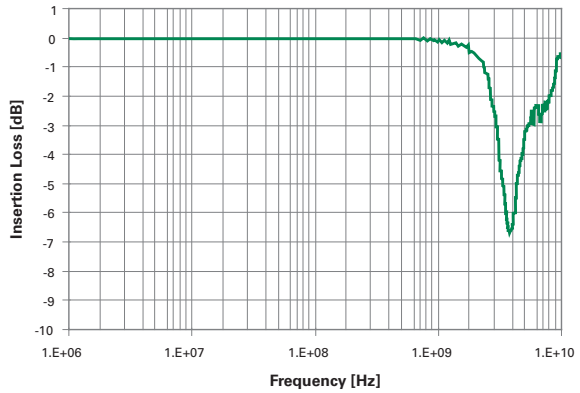
Parameter	Rating	Units
Storage Temperature Range	-65 to 150	°C
Maximum Junction Temperature	150	°C
Maximum Lead Temperature (Soldering 10s)	300	°C

Electrical Characteristics (T_{OP}=25°C)

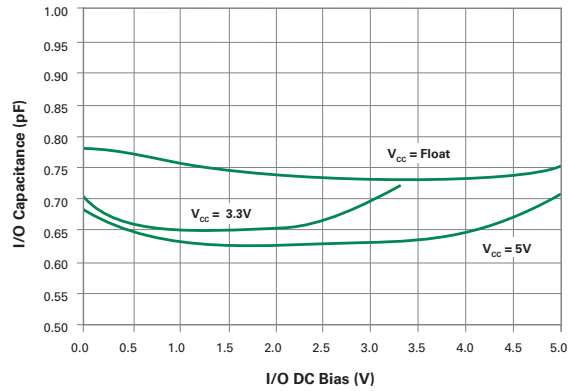
Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Zener Breakdown Voltage	V_{BR}	I_R=10µA	6.0			V
Reverse Leakage Current	I_{LEAK}	V_R=5V			0.5	µA
Clamp Voltage[1]	V_C	I_{PP}=1A, t_p=8/20µs, Fwd		10.0		V
		I_{PP}=2A, t_p=8/20µs, Fwd		11.8		V
ESD Withstand Voltage[1]	V_{ESD}	IEC61000-4-2 (Contact)	±8			kV
		IEC61000-4-2 (Air)	±15			kV
Diode Capacitance[1]	$C_{I/O-GND}$	Reverse Bias=0V		0.80		pF
		Reverse Bias=1.65V		0.65		pF
Diode Capacitance[1]	$C_{I/O-I/O}$	Reverse Bias=0V		0.35		pF

Note 1: Parameter is guaranteed by device characterization

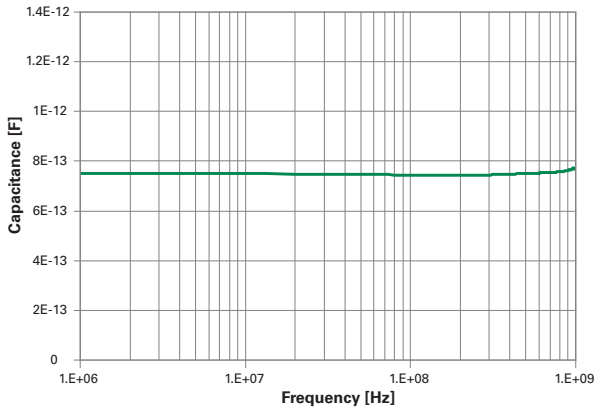
Insertion Loss (S21) I/O to GND



Capacitance vs. Bias Voltage

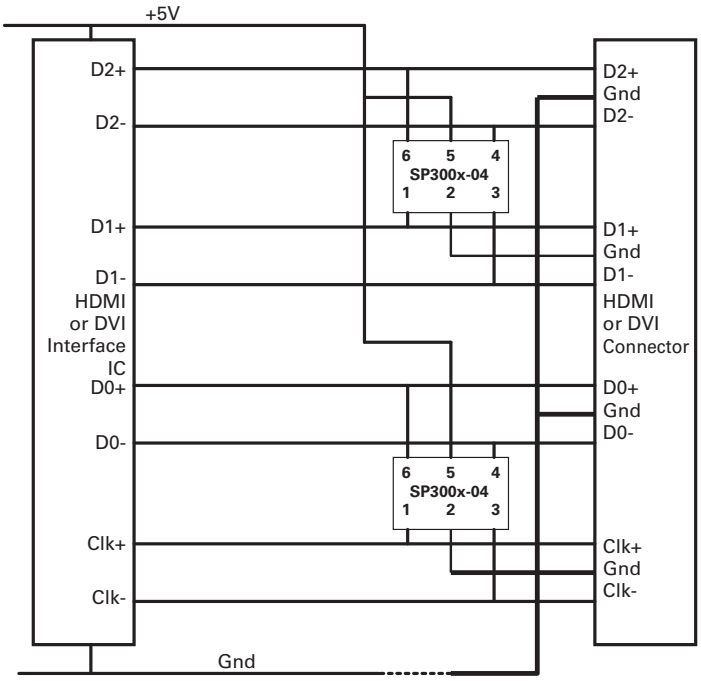


Capacitance vs. Frequency



Lead-Free/Green SP3003

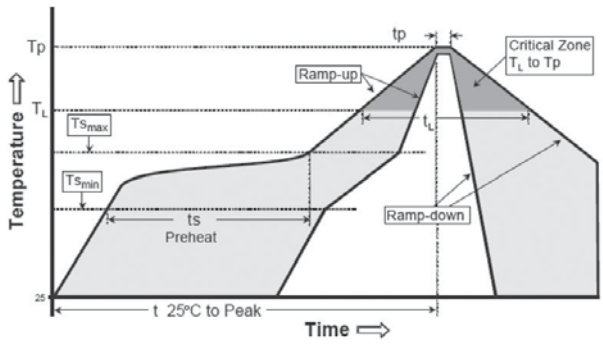
Application Example



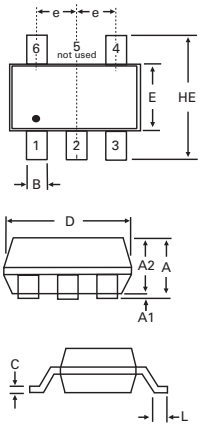
HDMI or DVI application example for the Littelfuse SP300x-04 protection devices. A single 4 channel SP300x-04 device can be used to protect four of the data lines in a HDMI/DVI interface. Two (2) SP300x-04 devices provide protection for the main data lines. Low voltage ASIC HDMI/DVI drivers can also be protected with the SP300x-04, the $+V_{CC}$ pins on the SP300x-04 can be substituted with a suitable bypass capacitor or in some backdrive applications the $+V_{CC}$ of the SP300x-04 can be floated or NC.

Soldering Parameters

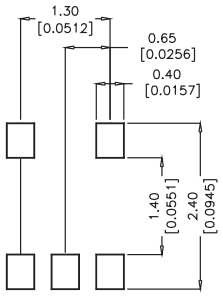
Reflow Condition		Pb – Free assembly
Pre Heat	-Temperature Min ($T_{s(min)}$)	150°C
	-Temperature Max ($T_{s(max)}$)	200°C
	-Time (min to max) (t_s)	60 – 180 secs
Average ramp up rate (Liquidus) Temp (T_L) to peak		3°C/second max
$T_{S(max)}$ to T_L - Ramp-up Rate		3°C/second max
Reflow	-Temperature (T_L) (Liquidus)	217°C
	-Temperature (t_L)	60 – 150 seconds
Peak Temperature (T_P)		$250^{+0/-5}$ °C
Time within 5°C of actual peak Temperature (t_p)		20 – 40 seconds
Ramp-down Rate		6°C/second max
Time 25°C to peak Temperature (T_P)		8 minutes Max.
Do not exceed		260°C



Package Dimensions — SC70-5

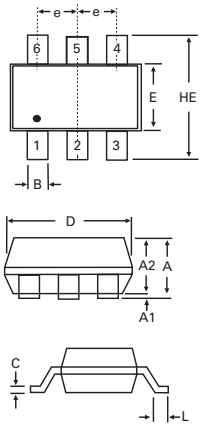


Solder Pad Layout

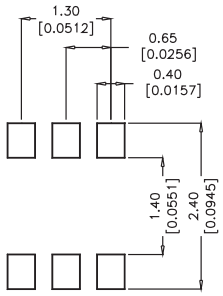


Package	SC70-5			
Pins	5			
JEDEC	MO-203 Issue A			
	Millimeters		Inches	
	Min	Max	Min	Max
A	0.80	1.10	0.031	0.043
A1	0.00	0.10	0.000	0.004
A2	0.70	1.00	0.028	0.039
B	0.15	0.30	0.006	0.012
c	0.08	0.25	0.003	0.010
D	1.85	2.25	0.073	0.089
E	1.15	1.35	0.045	0.053
e	0.65 BSC		0.026 BSC	
HE	2.00	2.40	0.079	0.094
L	0.26	0.46	0.010	0.018

Package Dimensions — SC70-6

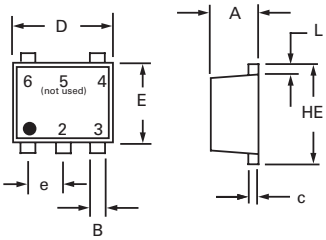


Solder Pad Layout

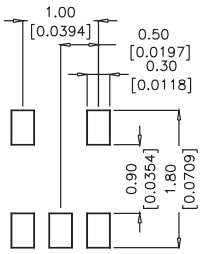


Package	SC70-6			
Pins	6			
JEDEC	MO-203 Issue A			
	Millimeters		Inches	
	Min	Max	Min	Max
A	0.80	1.10	0.031	0.043
A1	0.00	0.10	0.000	0.004
A2	0.70	1.00	0.028	0.039
B	0.15	0.30	0.006	0.012
c	0.08	0.25	0.003	0.010
D	1.85	2.25	0.073	0.089
E	1.15	1.35	0.045	0.053
e	0.65 BSC		0.026 BSC	
HE	2.00	2.40	0.079	0.094
L	0.26	0.46	0.010	0.018

Package Dimensions — SOT553

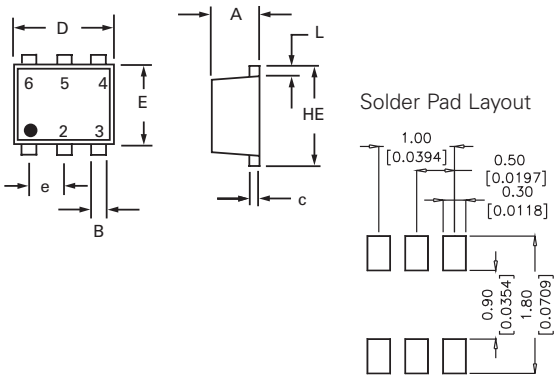


Solder Pad Layout



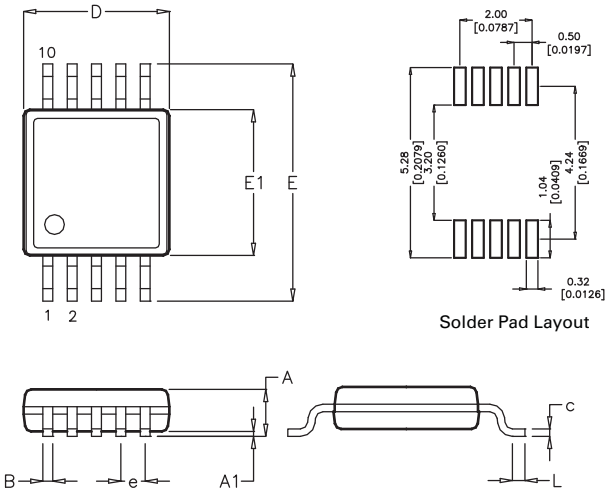
Package	SOT 553			
Pins	5			
	Millimeters		Inches	
	Min	Max	Min	Max
A	0.50	0.60	0.020	0.024
B	0.17	0.27	0.007	0.011
c	0.08	0.18	0.003	0.007
D	1.50	1.70	0.059	0.067
E	1.10	1.30	0.043	0.051
e	0.50 BSC		0.020 BSC	
L	0.10	0.30	0.004	0.012
HE	1.50	1.70	0.059	0.067

Package Dimensions — SOT563



Package	SOT 563			
Pins	6			
	Millimeters		Inches	
	Min	Max	Min	Max
A	0.50	0.60	0.020	0.024
B	0.17	0.27	0.007	0.011
c	0.08	0.18	0.003	0.007
D	1.50	1.70	0.059	0.067
E	1.10	1.30	0.043	0.051
e	0.50 BSC		0.020 BSC	
L	0.10	0.30	0.004	0.012
HE	1.50	1.70	0.059	0.067

Package Dimensions — MSOP10



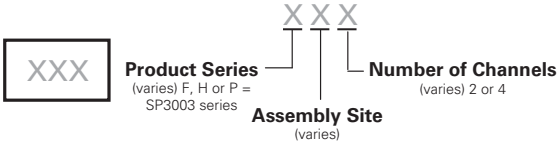
Package	MSOP10			
Pins	10			
	Millimeters		Inches	
	Min	Max	Min	Max
A	-	1.10	-	0.043
A1	0.00	0.15	0.000	0.006
B	0.17	0.27	0.007	0.011
c	0.08	0.23	0.003	0.009
D	2.90	3.10	0.114	0.122
E	4.67	5.10	0.184	0.200
E1	2.90	3.10	0.114	0.122
e	0.50 BSC		0.020 BSC	
HE	0.40	0.80	0.016	0.032

Part Numbering System

SP3003-04XTG

- Silicon Protection Array
- Series
- Number of Channels
  - -02 = 2 channel (SC70-5, SOT553 packages)
  - -04 = 4 channel (SC70-6, SOT563, MSOP-10 packages)
- Package
  - A = MSOP-10, 3000 quantity
  - J = SC70-5 or SC70-6, 3000 quantity
  - X = SOT553 or SOT563, 5000 quantity
- T= Tape & Reel
- G= Green

Part Marking System



Product Characteristics

Lead Plating	Matte Tin
Lead Material	Copper Alloy
Lead Coplanarity	0.0004 inches (0.102mm)
Subsitute Material	Silicon
Body Material	Molded Epoxy
Flammability	UL94-V-0

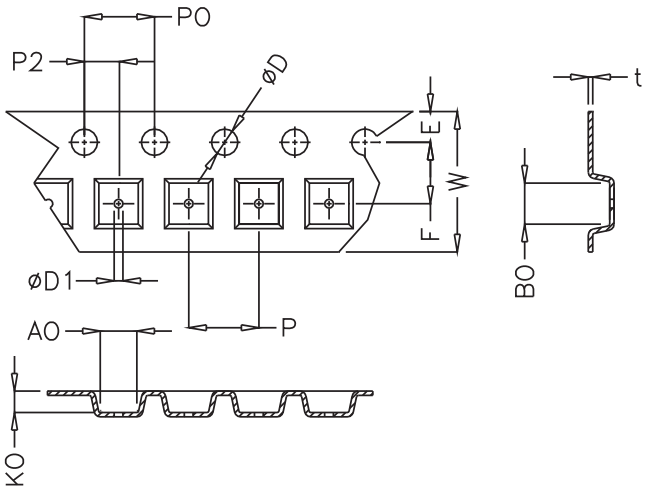
Notes :

1. All dimensions are in millimeters
2. Dimensions include solder plating.
3. Dimensions are exclusive of mold flash & metal burr.
4. All specifications comply to JEDEC SPEC MO-223 Issue A
5. Blo is facing up for mold and facing down for trim/form, i.e. reverse trim/form.
6. Package surface matte finish VDI 11-13.

Ordering Information

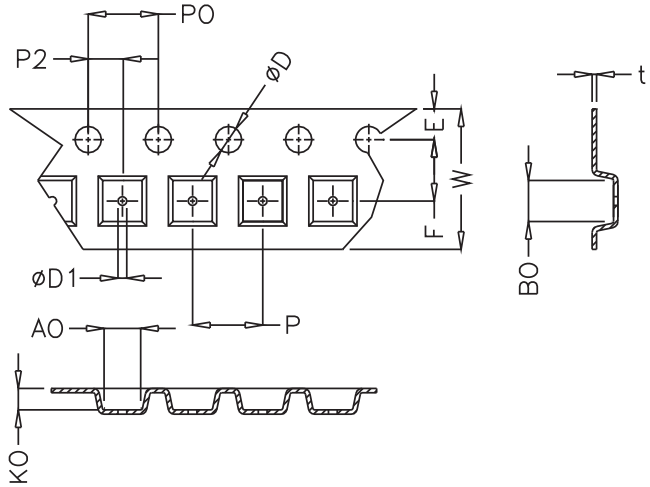
Part Number	Package	Marking	Min. Order Qty.
SP3003-02JTG	SC70-5	FX2	3000
SP3003-02XTG	SOT553	FX2	5000
SP3003-04ATG	MSOP-10	FX4	3000
SP3003-04JTG	SC70-6	FX4	3000
SP3003-04XTG	SOT563	FX4	5000

Embossed Carrier Tape & Reel Specifications - SC70-5 and SC70-6



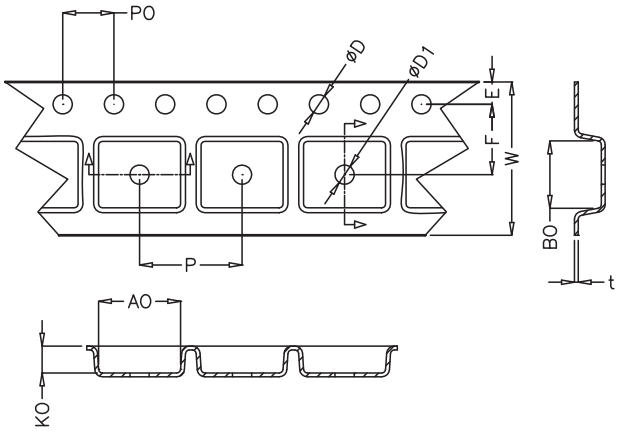
	Millimetres		Inches	
	Min	Max	Min	Max
E	1.65	1.85	0.064	0.072
F	3.45	3.55	0.135	0.139
P2	1.95	2.05	0.076	0.080
D	1.40	1.60	0.055	0.062
D1	1.00	1.25	0.039	0.049
P0	3.90	4.10	0.153	0.161
10P0	40.0+/- 0.20		1.574+/-0.007	
W	7.70	8.10	0.303	0.318
P	3.90	4.10	0.153	0.161
A0	2.14	2.34	0.084	0.092
B0	2.24	2.44	0.088	0.960
K0	1.12	1.32	0.044	0.052
t	0.27 max		0.010 max	

Embossed Carrier Tape & Reel Specifications - SOT553 and SOT563



	Millimetres		Inches	
	Min	Max	Min	Max
E	1.65	1.85	0.064	0.072
F	3.45	3.55	0.135	0.139
P2	1.95	2.05	0.076	0.080
D	1.40	1.60	0.055	0.062
D1	0.45	0.55	0.017	0.021
P0	3.90	4.10	0.153	0.161
10P0	40.0+/- 0.20		1.574+/-0.007	
W	7.70	8.10	0.303	0.318
P	3.90	4.10	0.153	0.161
A0	1.73	1.83	0.068	0.072
B0	1.73	1.83	0.068	0.072
K0	0.64	0.74	0.025	0.029
t	0.22 max		0.008 max	

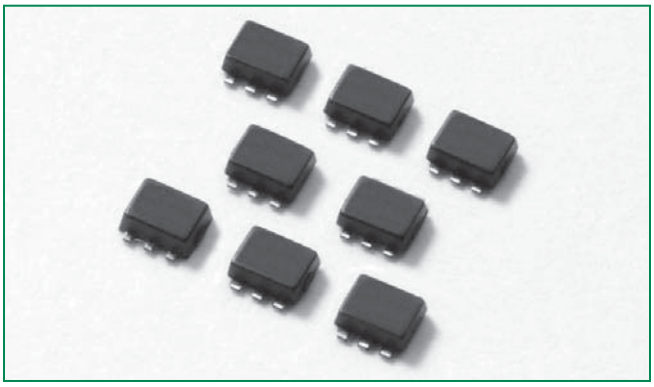
Embossed Carrier Tape & Reel Specification - MSOP-10



	Millimetres		Inches	
	Min	Max	Min	Max
E	1.65	1.85	0.064	0.072
F	5.40	5.60	0.212	0.220
D	1.50	1.60	0.059	0.062
D1	1.50 Min		0.059 Min	
P0	3.90	4.10	0.153	0.161
10P0	40.0+/- 0.20		1.574+/-0.007	
W	11.90	12.10	0.468	0.476
P	7.90	8.10	0.311	0.318
A0	5.20	5.40	0.204	0.212
B0	3.20	3.40	0.125	0.133
K0	1.20	1.40	0.047	0.055
t	0.30 +/- 0.05		0.011+/- 0.001	

RoHS Pb GREEN SP3004 Lead-Free/Green Series

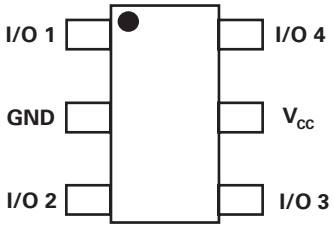
Scheduled for Release Q3/2008



Description

The SP3004 has ultra low capacitance rail-to rail diodes with an additional zener diode fabricated in a proprietary silicon avalanche technology to protect each I/O pin providing a high level of protection for electronic equipment that may experience destructive electrostatic discharges (ESD). These robust diodes can safely absorb repetitive ESD strikes at the maximum level (Level 4) specified in the IEC 61000-4-2 international standard without performance degradation. Their very low loading capacitance also makes them ideal for protecting high speed signal pins such as HDMI, DVI, USB2.0, and IEEE 1394.

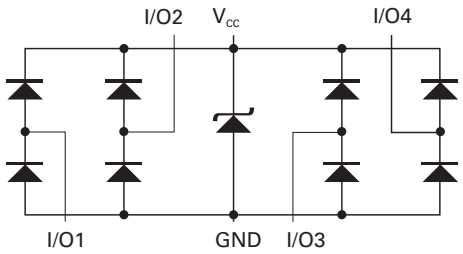
Pinout



Features

- Low capacitance of 0.85pF (TYP) per I/O
- ESD protection of ±12kV contact discharge, ±15kV air discharge, (IEC61000-4-2)
- EFT protection, IEC61000-4-4, 40A (5/50 ns)
- Low leakage current of 0.5µA (MAX) at 5V
- Small SOT563 package saves board space

Functional Block Diagram



Applications

- Computer Peripherals
- Mobile Phones
- PDA's
- Digital Cameras
- Network Hardware/Ports
- Test Equipment
- Medical Equipment

Absolute Maximum Ratings

Symbol	Parameter	Value	Units
I_P	Peak Current (t_p=8/20µs)	4	A
T_{OP}	Operating Temperature	-40 to 85	°C
T_{STOR}	Storage Temperature	-50 to 150	°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Thermal Information

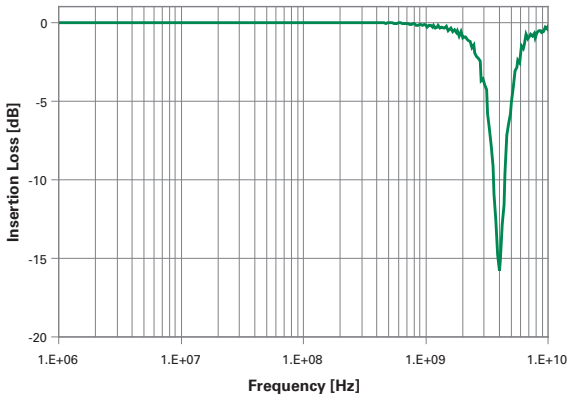
Parameter	Rating	Units
Storage Temperature Range	-65 to 150	°C
Maximum Junction Temperature	150	°C
Maximum Lead Temperature (Soldering 10s)	300	°C

Electrical Characteristics (T_{OP}=25°C)

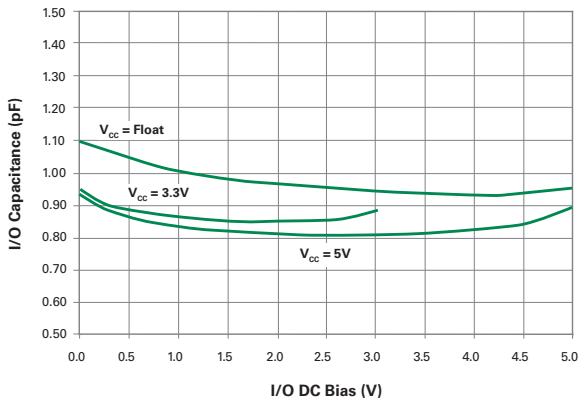
Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Zener Breakdown Voltage	V_{BR}	I_R=10µA	6.0			V
Reverse Leakage Current	I_{LEAK}	V_R=5V			0.5	µA
Clamp Voltage[1]	V_C	I_{PP}=1A, t_p=8/20µs, Fwd		10.0		V
		I_{PP}=2A, t_p=8/20µs, Fwd		11.8		V
ESD Withstand Voltage[1]	V_{ESD}	IEC61000-4-2 (Contact)	±12			kV
		IEC61000-4-2 (Air)	±15			kV
Diode Capacitance[1]	$C_{I/O-GND}$	Reverse Bias=0V		1.1		pF
		Reverse Bias=1.65V		0.85		pF
Diode Capacitance[1]	$C_{I/O-I/O}$	Reverse Bias=0V		0.5		pF

Note : [1] Parameter is guaranteed by device characterization

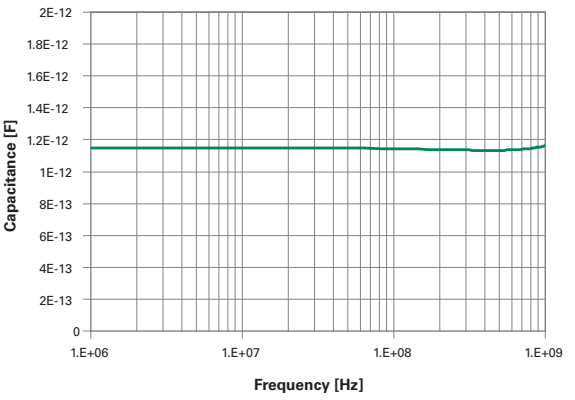
Insertion Loss (S21) I/O to GND



Capacitance vs. Bias Voltage

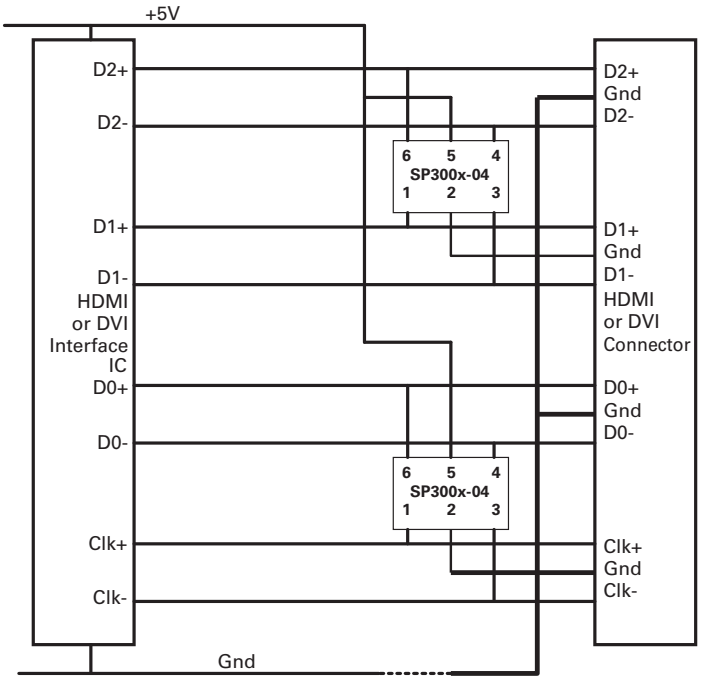


Capacitance vs. Frequency



Lead-Free/Green SP3004

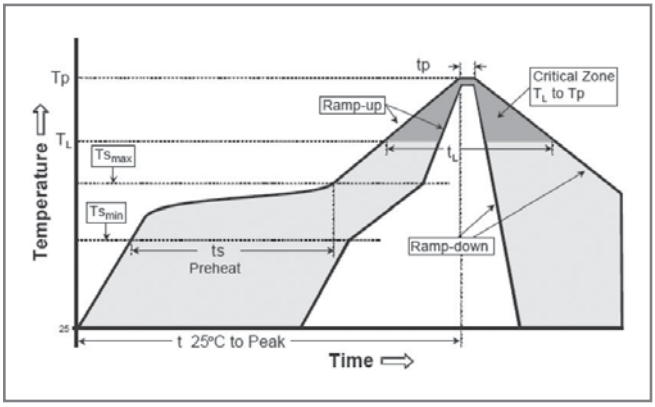
Application Example



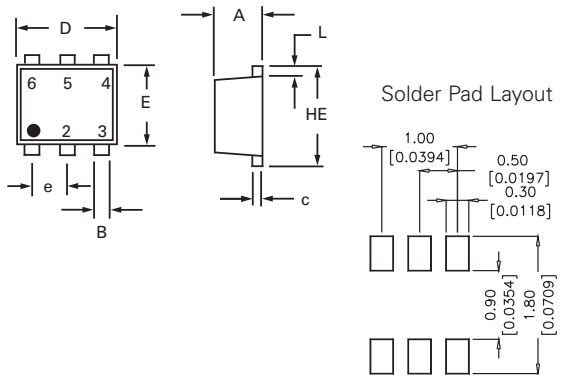
HDMI or DVI application example for the Littelfuse SP300x-04 protection devices. A single 4 channel SP300x-04 device can be used to protect four of the data lines in a HDMI/DVI interface. Two (2) SP300x-04 devices provide protection for the main data lines. Low voltage ASIC HDMI/DVI drivers can also be protected with the SP300x-04, the $+V_{CC}$ pins on the SP300x-04 can be substituted with a suitable bypass capacitor or in some backdrive applications the $+V_{CC}$ of the SP300x-04 can be floated or NC.

Soldering Parameters

Reflow Condition		Pb – Free assembly
Pre Heat	-Temperature Min ($T_{s(min)}$)	150°C
	-Temperature Max ($T_{s(max)}$)	200°C
	-Time (min to max) (t_s)	60 – 180 secs
Average ramp up rate (Liquidus) Temp (T_L) to peak		3°C/second max
$T_{S(max)}$ to T_L - Ramp-up Rate		3°C/second max
Reflow	-Temperature (T_L) (Liquidus)	217°C
	-Temperature (t_L)	60 – 150 seconds
Peak Temperature (T_P)		$250^{+0/-5}$ °C
Time within 5°C of actual peak Temperature (t_p)		20 – 40 seconds
Ramp-down Rate		6°C/second max
Time 25°C to peak Temperature (T_P)		8 minutes Max.
Do not exceed		260°C

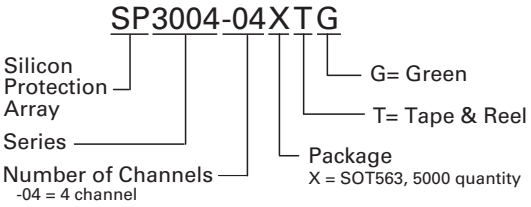


Package Dimensions - SOT563

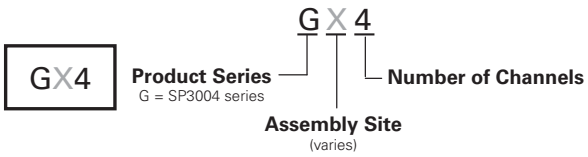


Package	SOT 563			
Pins	6			
	Millimeters		Inches	
	Min	Max	Min	Max
A	0.50	0.60	0.020	0.024
B	0.17	0.27	0.007	0.011
c	0.08	0.18	0.003	0.007
D	1.50	1.70	0.059	0.067
E	1.10	1.30	0.043	0.051
e	0.50 BSC		0.020 BSC	
L	0.10	0.30	0.004	0.012
HE	1.50	1.70	0.059	0.067

Part Numbering System



Part Marking System



Product Characteristics

Lead Plating	Matte Tin
Lead Material	Copper Alloy
Lead Coplanarity	0.0004 inches (0.102mm)
Subsitute Material	Silicon
Body Material	Molded Epoxy
Flammability	UL94-V-0

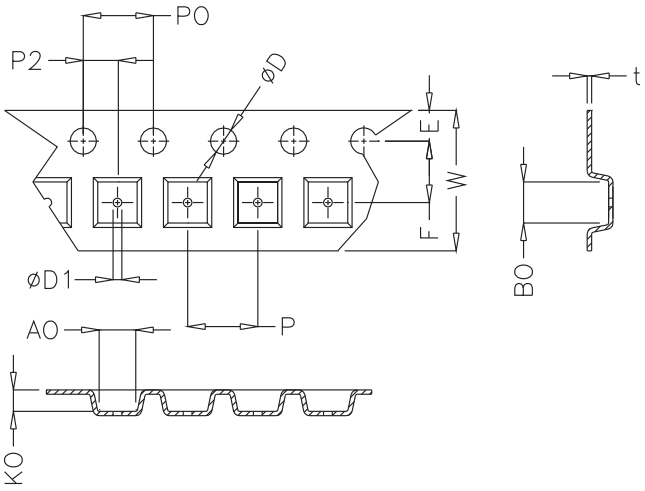
Notes :

1. All dimensions are in millimeters
2. Dimensions include solder plating.
3. Dimensions are exclusive of mold flash & metal burr.
4. All specifications comply to JEDEC SPEC MO-223 Issue A
5. Blo is facing up for mold and facing down for trim/form, i.e. reverse trim/form.
6. Package surface matte finish VDI 11-13.

Ordering Information

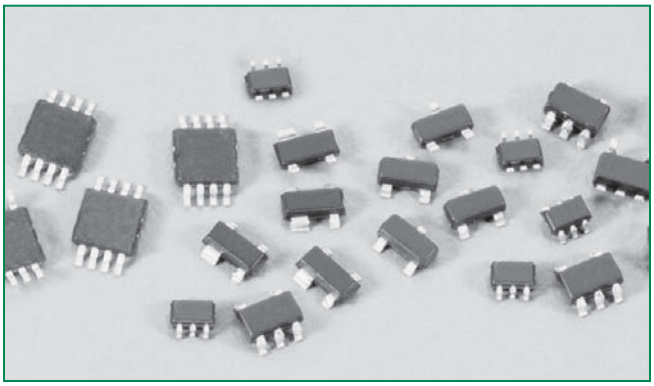
Part Number	Package	Marking	Min. Order Qty.
SP3004-04XTG	SOT563	GX4	5000

Embossed Carrier Tape & Reel Specification - SOT563



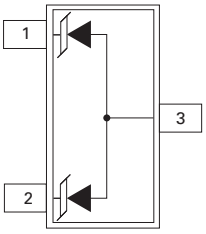
	Millimetres		Inches	
	Min	Max	Min	Max
E	1.65	1.85	0.064	0.072
F	3.45	3.55	0.135	0.139
P2	1.95	2.05	0.076	0.080
D	1.40	1.60	0.055	0.062
D1	0.45	0.55	0.017	0.021
P0	3.90	4.10	0.153	0.161
10P0	40.0+/- 0.20		1.574+/-0.007	
W	7.70	8.10	0.303	0.318
P	3.90	4.10	0.153	0.161
A0	1.73	1.83	0.068	0.072
B0	1.73	1.83	0.068	0.072
K0	0.64	0.74	0.025	0.029
t	0.22 max		0.008 max	

RoHS Pb GREEN SP050xBA Lead-Free/Green Series

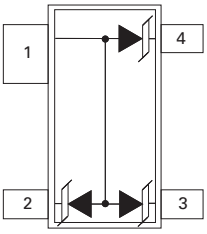


Pinout

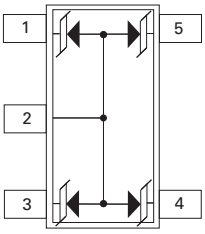
SP0502BAHTG
SP0502BAJTG



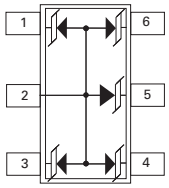
SP0503BAHTG



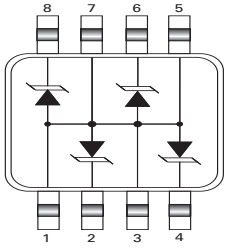
SP0504BAHTG
SP0504BAJTG



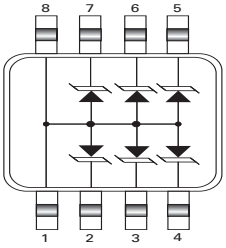
SP0505BAHTG
SP0505BAJTG



SP0504BAATG



SP0506BAATG



Description

The surface mount family of arrays are designed to suppress ESD and other transient overvoltage events. These arrays are used to meet the International Electrotechnical Compatibility (IEC transient immunity standards IEC 61000-4-2 for Electrostatic Discharge Requirements). The series are used to help protect sensitive digital or analog input circuits on data, signal, or control lines with voltage levels up to 5VDC.

The monolithic silicon arrays are comprised of specially designed structures for transient voltage suppression(TVS). The size and shape of these structures have be tailored for transient protection. The low capacitance and clamp voltage are ideal for high speed signal line protection.

Features

- An Array of 2, 3, 4, 5 or 6 TVS Avalanche Diodes in a ultra small SC70, SOT-23, SOT-143, MSOP or TSSOP packages
- ESD Capability Standards
  - IEC 61000-4-2, Direct Discharge ..... 20kV (Level 4)
  - IEC 61000-4-2, Air Discharge..... 30kV (Level 4)
  - MIL STD 883 3015.7.....30kV
- Input Protection for Applications Up to 5VDC
- Fast Response Time.....<1ns
- Low Input Capacitance.....30pF Typical
- Operating Temperature Range..... -40°C to 85°C

Applications

- Mobile phone handsets
- Personal Digital Assistants (PDA)
- Portable handheld equipment (Laptop, Palmtop computers)
- Computer port, keyboard (USB1.1)
- Digital still cameras
- Digital video cameras
- MP3 players

Absolute Maximum Ratings

Parameter	Rating	Units
Storage Temperature Range	-65 to + 150	°C
Package Power Dissipation		
SC70	0.2	W
SOT23-3, SOT23-5, SOT23-6, SOT143	0.225	W
TSSOP, MSOP	0.5	W

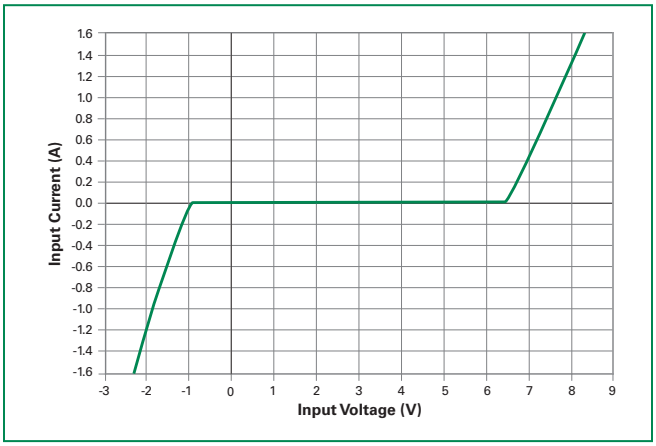
Electrical Characteristics T_A = +25°C, Unless Otherwise Specified

Parameter	Test Conditions	Min	Typ	Max	Units
Reverse Standoff Voltage	I = 10µA	5.5	-	-	V
Reverse Standoff Leakage Current	V = 5.0V		1	100	nA
Signal Clamp Voltage					
Positive	I = 10mA	5.6	6.8	8	V
Negative	I = 10mA	-1.2	-0.8	-0.4	V
Clamp Voltage during ESD					
MIL-STD-883 Method 3015 (HBM) test					
+ 8kV			12		V
- 8kV			-8		V
ESD Test Level (1)					
IEC-61000-2, Contact discharge		20			kV
MIL-STD-883 Method 3015 (HBM)		30			kV
Capacitance	2.5V @ 1Mhz		30		pF
Turn on/off Time			<1		ns
Temperature Range					
Operating		-40		85	°C
Storage		-65		150	°C
Diode Dynamic Resistance					
Forward Conduction			1.0		Ω
Reverse Conduction			1.4		Ω

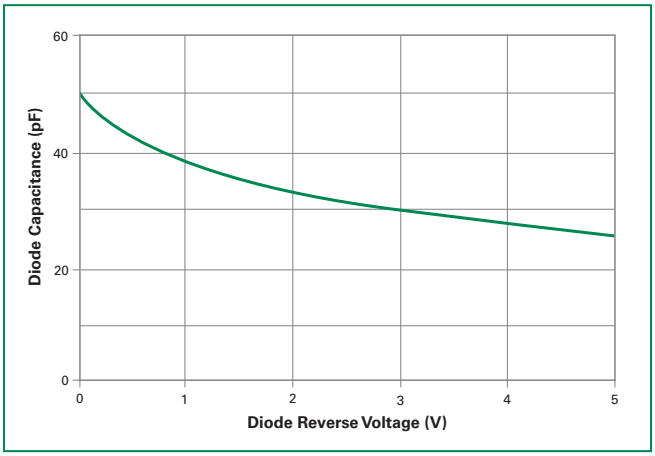
Note:
(1) ESD voltage applied between channel pins and ground, one pin at a time; all other channel pins are open; all ground pins are grounded.

Typical Input VI Characteristics

(Pulse-mode measurements, pulse width = 0.7 mS nominal)

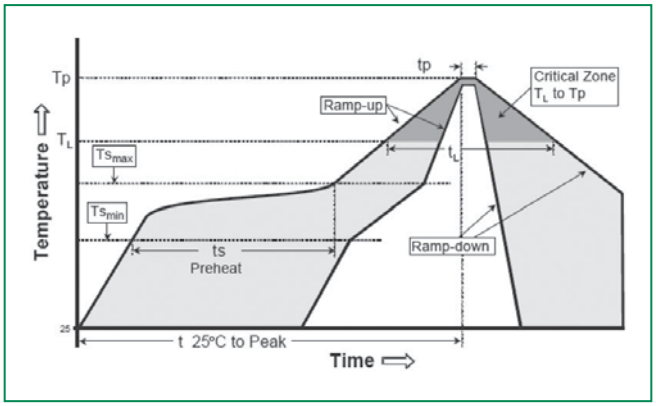


Typical Diode Capacitance vs. Reverse Voltage



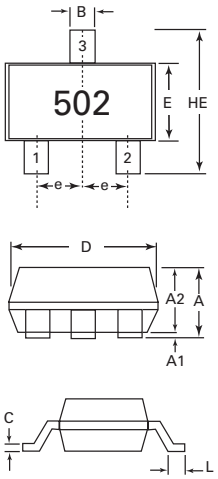
Soldering Parameters - Wave Soldering

Reflow Condition		Pb – Free assembly
Pre Heat	-Temperature Min ($T_{s(min)}$)	150°C
	-Temperature Max ($T_{s(max)}$)	200°C
	-Time (min to max) (t_s)	60 – 180 secs
Average ramp up rate (Liquidus) Temp (T_L) to peak		5°C/second max
$T_{S(max)}$ to T_L - Ramp-up Rate		5°C/second max
Reflow	-Temperature (T_L) (Liquidus)	217°C
	-Temperature (t_L)	60 – 150 seconds
Peak Temperature (T_P)		$250^{+0/-5}$ °C
Time within 5°C of actual peak Temperature (t_p)		20 – 40 seconds
Ramp-down Rate		5°C/second max
Time 25°C to peak Temperature (T_P)		8 minutes Max.
Do not exceed		260°C



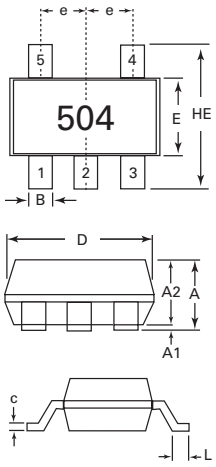
Lead-Free/Green SP050xBA

Package Dimensions - SC70



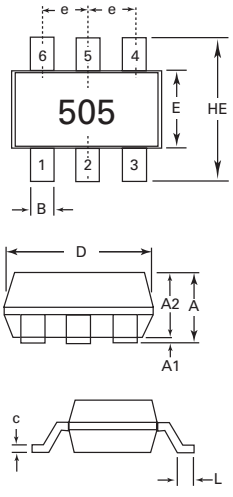
SP0502BAJTG - SC70-3

Package	SC70-3			
Pins	3			
JEDEC	MO-203 Issue A			
	Millimeters		Inches	
	Min	Max	Min	Max
A	0.80	1.10	0.031	0.043
A1	0.00	0.10	0.00	0.004
A2	0.70	1.00	0.028	0.039
B	0.15	0.30	0.006	0.012
c	0.08	0.25	0.003	0.010
D	1.85	2.25	0.073	0.089
E	1.15	1.35	0.045	0.053
e	0.66 BSC		0.026 BSC	
HE	2.00	2.40	0.079	0.094
L	0.26	0.46	0.010	0.018



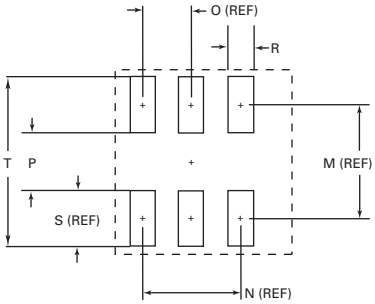
SP0504BAJTG - SC70-5

Package	SC70-5			
Pins	5			
JEDEC	MO-203 Issue A			
	Millimeters		Inches	
	Min	Max	Min	Max
A	0.80	1.10	0.03	0.043
A1	0.00	0.10	0.00	0.004
A2	0.70	1.00	0.028	0.039
B	0.15	0.30	0.006	0.012
c	0.08	0.25	0.003	0.010
D	1.85	2.25	0.073	0.089
E	1.15	1.35	0.045	0.053
e	0.65 BSC		0.026 BSC	
HE	2.00	2.40	0.079	0.094
L	0.26	0.46	0.010	0.018



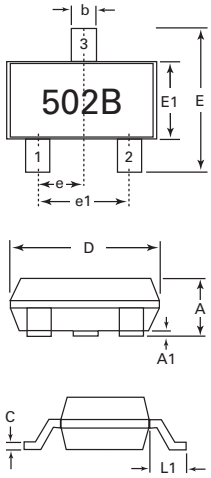
SP0505BAJTG - SC70-6

Recommended Pad Layout



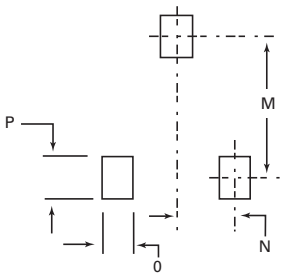
Package	SC70-6			
Pins	6			
JEDEC	MO-203 Issue A			
	Millimeters		Inches	
	Min	Max	Min	Max
A	0.80	1.10	0.031	0.043
A1	0.00	0.10	0.00	0.004
A2	0.70	1.00	0.028	0.039
B	0.15	0.30	0.006	0.012
c	0.08	0.25	0.003	0.010
D	1.85	2.25	0.073	0.089
E	1.15	1.35	0.045	0.053
e	0.65 BSC		0.026 BSC	
HE	2.00	2.40	0.079	0.094
L	0.26	0.46	0.010	0.018
M	-	1.60	-	0.063
N	-	1.30	-	0.052
O	-	0.65	-	0.026
P	-	0.70	-	0.058
R	-	0.35	-	0.014
S	-	0.90	-	0.035
T	-	2.50	-	0.098

Package Dimensions - SOT23

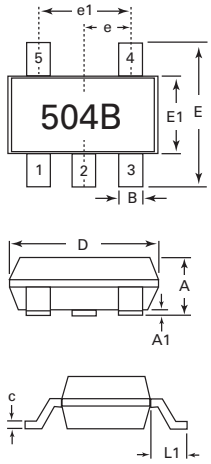


SP0502BAHT - SOT23-3

Recommended Pad Layout

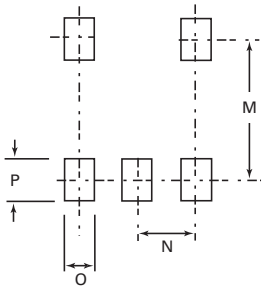


Package	SOT23-3			
Pins	3			
JEDEC	TO-236			
	Millimeters		Inches	
	Min	Max	Min	Max
A	0.89	1.12	0.035	0.044
A1	0.01	0.1	0.0004	0.004
b	0.3	0.5	0.012	0.020
c	0.08	0.2	0.003	0.008
D	2.8	3.04	0.110	0.120
E	2.1	2.64	0.083	0.104
E1	1.2	1.4	0.047	0.055
e	0.95 BSC		0.95 BSC	
e1	1.90 BSC		1.90 BSC	
L1	0.54 REF		0.54 REF	
M		2.29		.090
N		0.95		.0375
O		0.78		.030TYP
P		0.78		.030TYP

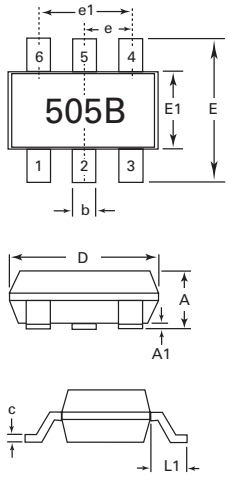


SP0504BAHTG - SOT23-5

Recommended Pad Layout

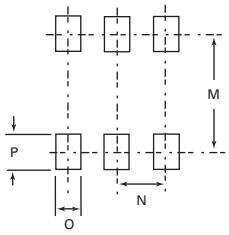


Package	SOT23-5			
Pins	5			
JEDEC	MO-178			
	Millimeters		Inches	
	Min	Max	Min	Max
A	-	1.45	-	0.057
A1	0	0.15	0	0.006
b	0.3	0.5	0.012	0.020
c	0.08	0.22	0.003	0.009
D	2.75	3.05	0.108	0.120
E	2.6	3.0	0.102	0.118
E1	1.45	1.75	0.057	0.069
e	0.95 BSC		0.95 BSC	
e1	1.90 BSC		1.90 BSC	
L1	0.60 REF		0.60 REF	
M		2.59		.102
N		0.95		.038
O		0.69		.027TYP
P		0.99		.039TYP



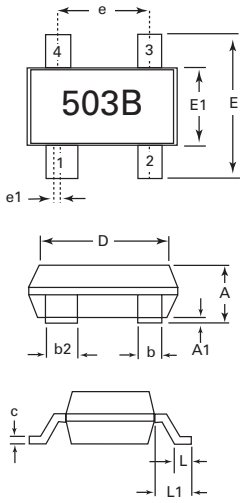
SP0505BAHTG - SOT23-6

Recommended Pad Layout



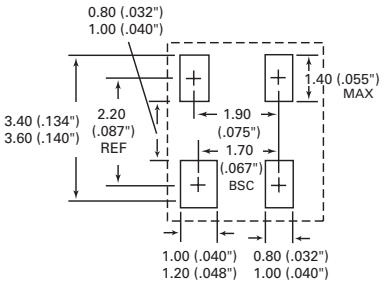
Package	SOT23-6			
Pins	6			
JEDEC	MO-178			
	Millimeters		Inches	
	Min	Max	Min	Max
A	-	1.45	-	0.057
A1	0	0.15	0	0.006
b	0.3	0.5	0.012	0.020
c	0.08	0.22	0.003	0.009
D	2.75	3.05	0.108	0.120
E	2.6	3.0	0.102	0.118
E1	1.45	1.75	0.057	0.069
e	0.95 BSC		0.95 BSC	
e1	1.90 BSC		1.90 BSC	
L1	0.60 REF		0.60 REF	
M		2.59		.102
N		0.95		0.038
O		0.69		.027TYP
P		0.99		.039TYP

Package Dimensions - SOT143



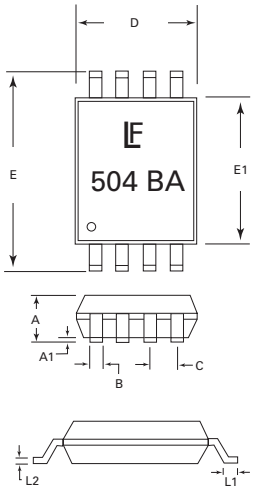
SP0503BAHTG - SOT143-4

Recommended Pad Layout



Package	SOT143-4			
Pins	4			
JEDEC	TO-253			
	Millimeters		Inches	
	Min	Max	Min	Max
A	0.08	1.22	0.031	0.048
A1	0.05	0.15	0.002	0.006
b	0.30	0.50	0.012	0.019
b2	0.76	0.89	0.030	0.035
c	0.08	0.20	0.003	0.008
D	2.80	3.04	0.110	0.119
E	2.10	2.64	0.082	0.103
E1	1.20	1.40	0.047	0.055
e	1.92 BSC		0.076 BSC	
e1	0.20 BSC		0.008 BSC	
L	0.4	0.6	0.016	0.024
L1	0.550 REF		0.022 REF	

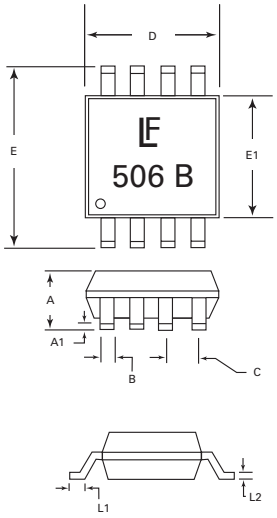
Package Dimensions - TSSOP



SP0504BAATG - TSSOP-8

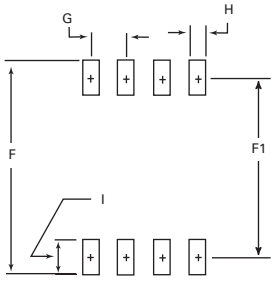
Package	TSSOP-8			
Pins	8			
	Millimeters		Inches	
	Min	Max	Min	Max
D	2.90	3.10	.144	.122
E	6.40 REF		.252 REF	
E1	4.29	4.50	.17	.18
A	1.194 REF		.047 REF	
A1	0.051	0.152	.002	0.006
B	-	0.30	-	.12TYP
C	-	0.66	-	.26TYP
L1	0.51	0.76	.020	.030
L2	0.102	0.203	.004	.008

Package Dimensions - MSOP



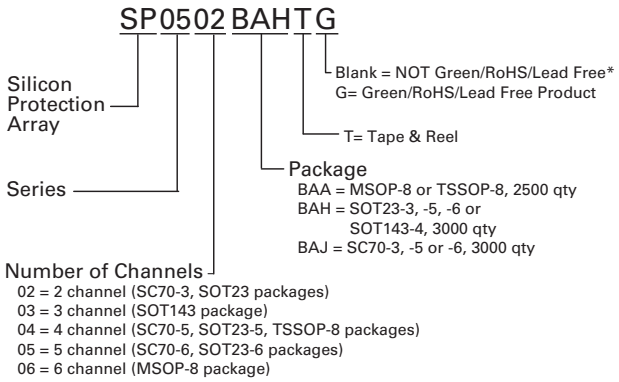
SP0506BAATG - MSOP-8

Recommended Pad Layout



Package	MSOP-8			
Pins	8			
	Millimeters		Inches	
	Min	Max	Min	Max
D	2.90	3.10	.144	.122
E	4.78	4.98	.188	.196
E1	2.90	3.10	.114	.122
A	0.87	1.17	.034	.046
A1	0.05	0.25	.002	0.10
B	-	0.30TYP	-	.12TYP
C	-	0.65TYP	-	.25TYP
L1	0.52	0.54	.017	.025
L2	-	0.18TYP	-	.007TYP
F	-	5.28	-	.208
F1	-	4.24	-	.167
G	-	0.65	-	.0256
H	-	0.38	-	.015
I	-	1.04	-	.041

Part Numbering System



Product Characteristics

Lead Plating	"G" Green version - Matte Tin (Sn); *Non-Green version - Tin Lead
Lead Material	Copper Alloy
Lead Coplanarity	0.004 inches (0.102mm)
Subsitute Material	Silicon
Body Material	Molded Epoxy
Flammability	UL94-V-0

Notes:

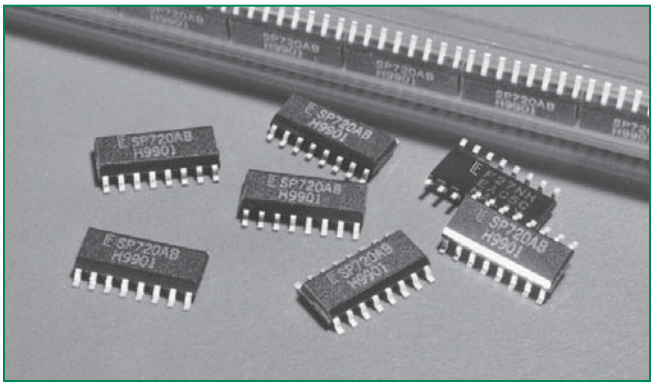
1. All dimensions are in millimeters.
2. Dimensions include solder plating.
3. Dimensions are exclusive of mold flash & metal burr.
4. All specifications comply to JEDEC SPEC MO-203 ISSUE A.
5. Blo is facing up for mold and facing down for trim/form, i.e. reverse trim/form.
6. Package surface matte finish VDI 11-13.

Ordering Information

*NOTE: To order NON-Green/RoHS/Lead Free version of product, remove "G" at the end of part number.

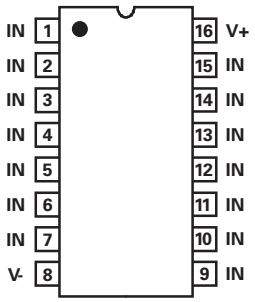
Part Number	CH	Package Type	Quantity Per Reel
SP0502BAHTG	2	SOT23-3	3000
SP0503BAHTG	3	SOT143-4	3000
SP0504BAHTG	4	SOT23-5	3000
SP0505BAHTG	5	SOT23-6	3000
SP0504BAATG	4	TSSOP-8	2500
SP0506BAATG	6	MSOP-8	2500
SP0502BAJTG	2	SC70-3	3000
SP0504BAJTG	4	SC70-5	3000
SP0505BAJTG	5	SC70-6	3000

RoHS Pb GREEN SP720 Lead-Free/Green Series

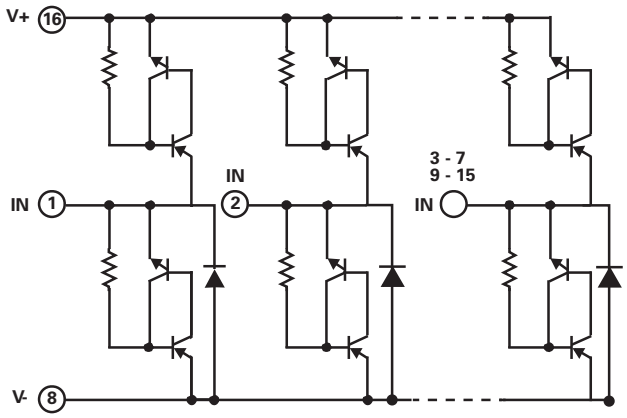


Pinout

SP720 (PDIP, SOIC)
TOP VIEW



Functional Block Diagram



Description

The SP720 is an array of SCR/Diode bipolar structures for ESD and over-voltage protection to sensitive input circuits. The SP720 has 2 protection SCR/Diode device structures per input. A total of 14 available inputs can be used to protect up to 14 external signal or bus lines. Over-voltage protection is from the IN (pins 1-7 and 9-15) to V+ or V-.

The SCR structures are designed for fast triggering at a threshold of one $+V_{BE}$ diode threshold above V+ (Pin 16) or a $-V_{BE}$ diode threshold below V- (Pin 8). From an IN input, a clamp to V+ is activated if a transient pulse causes the input to be increased to a voltage level greater than one V_{BE} above V+. A similar clamp to V- is activated if a negative pulse, one V_{BE} less than V-, is applied to an IN input. Standard ESD Human Body Model (HBM) Capability is:

Features

- ESD Interface Capability for HBM Standards
  - MIL STD 3015.7 ..... 15kV
  - IEC 61000-4-2, Direct Discharge,
  - Single Input ..... 4kV (Level 2)
  - Two Inputs in Parallel ..... 8kV (Level 4)
  - IEC 61000-4-2, Air Discharge ..... 15kV (Level 4)
- High Peak Current Capability
  - IEC 61000-4-5 (8/20µs) ..... ±3A
  - Single Pulse, 100µs Pulse Width ..... ±2A
  - Single Pulse, 4µs Pulse Width ..... ±5A
- Designed to Provide Over-Voltage Protection
  - Single-Ended Voltage Range to ..... +30V
  - Differential Voltage Range to ..... ±15V
- Fast Switching ..... 2ns Risetime
- Low Input Leakages ..... 1nA at 25° (Typ)
- Low Input Capacitance ..... 3pF (Typ)
- An Array of 14 SCR/Diode Pairs
- Operating Temperature Range ..... -40°C to 105°C

Applications

- Microprocessor/Logic Input Protection
- Data Bus Protection
- Analog Device Input Protection
- Voltage Clamp

Absolute Maximum Ratings

Parameter	Rating	Units
Continuous Supply Voltage, (V+) - (V-)	+35	V
Forward Peak Current, I_{IN} to V_{CC}, I_{IN} to GND (Refer to Figure 6)	±2A, 100µs	V

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Note:
ESD Ratings and Capability - See Figure 1, Table 1
Load Dump and Reverse Battery (Note 2)

Thermal Information

Parameter	Rating	Units
Thermal Resistance (Typical, Note 1)	θ_{JA}	°C/W
PDIP Package	90	°C/W
SOIC Package	130	°C/W
Maximum Storage Temperature Range	-65 to 150	°C
Maximum Junction Temperature (Plastic Package)	150	°C
Maximum Lead Temperature (Soldering 10s) (SOIC Lead Tips Only)	300	°C

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Characteristics T_A = -40°C to 105°C, V_{IN} = 0.5V_{CC} , Unless Otherwise Specified

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Operating Voltage Range, V_{SUPPLY} = [(V+) - (V-)]	V_{SUPPLY}		-	2 to 30	-	V
Forward Voltage Drop:		I_{IN} = 1A (Peak Pulse)				
IN to V-	V_{FWDL}		-	2	-	V
IN to V+	V_{FWDH}		-	2	-	V
Input Leakage Current	I_{IN}		-20	5	20	nA
Quiescent Supply Current	$I_{QUIESCENT}$		-	50	200	nA
Equivalent SCR ON Threshold		Note 3	-	1.1	-	V
Equivalent SCR ON Resistance		V_{FWD}/I_{FWD}; Note 3	-	1	-	Ω
Input Capacitance	C_{IN}		-	3	-	pF
Input Switching Speed	t_{ON}		-	2	-	ns

Notes:

2. In automotive and battery operated systems, the power supply lines should be externally protected for load dump and everse battery V+ and V- pins are connected to the same supply voltage source as the device or control line under protection, a current limiting resistor should be connected in series between the external supply and the SP720 supply pins to limit reverse battery current to within the rated maximum limits. Bypass capacitors of typically 0.01µF or larger from the V+ and V- pins to ground are recommended.
3. Refer to the Figure 3 graph for definitions of equivalent "SCR ON Threshold" and "SCR ON Resistance." These characteristics are given here for thumb-rule nformation to determine peak current and dissipation under EOS conditions.

ESD Capability

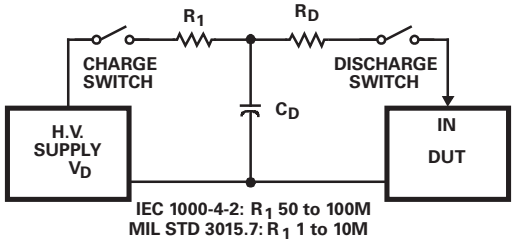
ESD capability is dependent on the application and defined test standard. The evaluation results for various test standards and methods based on Figure 1 are shown in Table 1.

For the "Modified" MIL-STD-3015.7 condition that is defined as an "in-circuit" method of ESD testing, the V+ and V- pins have a return path to ground and the SP720 ESD capability is typically greater than 15kV from 100pF through 1.5kΩ. By strict definition of MIL-STD-3015.7 using "pin-to-pin" device testing, the ESD voltage capability is greater than 6kV. The MIL-STD-3015.7 results were determined from AT&T ESD Test Lab measurements.

The HBM capability to the IEC 61000-4-2 standard is greater than 15kV for air discharge (Level 4) and greater than 4kV for direct discharge (Level 2). Dual pin capability (2 adjacent pins in parallel) is well in excess of 8kV (Level 4).

For ESD testing of the SP720 to EIAJ IC121 Machine Model (MM) standard, the results are typically better than 1kV from 200pF with no series resistance.

ELECTROSTATIC DISCHARGE TEST

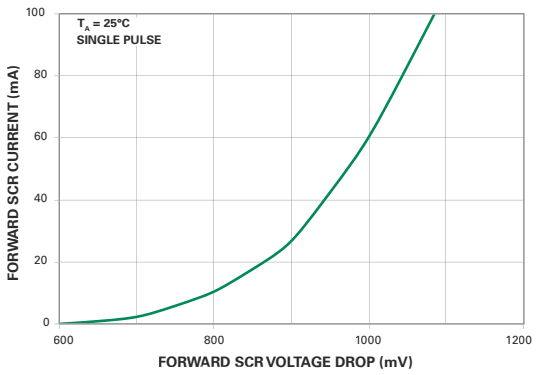


IEC 1000-4-2: R_1 50 to 100M
MIL STD 3015.7: R_1 1 to 10M

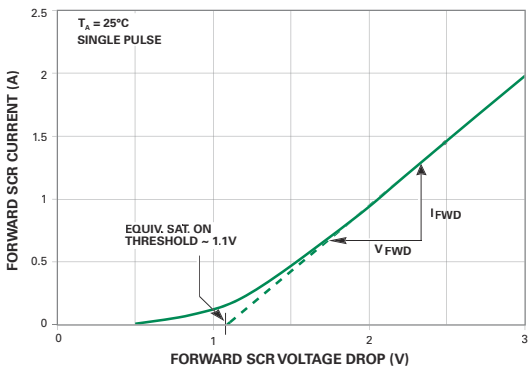
ESD Test Conditions

STANDARD	TYPE/MODE	R_D	C_D	$\pm V_D$
MIL STD 3015.7	Modified HBM	1.5kΩ	100pF	15kV
	Standard HBM	1.5kΩ	100pF	6kV
IEC 61000-4-2	HBM, Air Discharge	330Ω	150pF	15kV
	HBM, Direct Discharge	330Ω	150pF	4kV
	HBM, Direct Discharge, Two Parallel Input Pins	330Ω	150pF	8kV
EIAJ IC121	Machine Model	0kΩ	200pF	1kV

Low Current SCR Forward Voltage Drop Curve



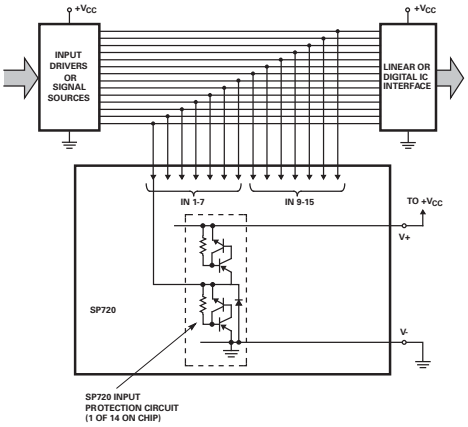
High Current SCR Forward Voltage Drop Curve



Lead-Free/Green SP720

Typical Application of the SP720

• (Application as an Input Clamp for Over-voltage, greater than $1V_{BE}$ Above V+ or less than $-1V_{BE}$ below V-)



Peak Transient Current Capability for Long Duration Surges

The peak transient current capability rises sharply as the width of the current pulse narrows. Destructive testing was done to fully evaluate the SP720's ability to withstand a wide range of transient current pulses. The circuit used to generate current pulses is shown in Figure 5.

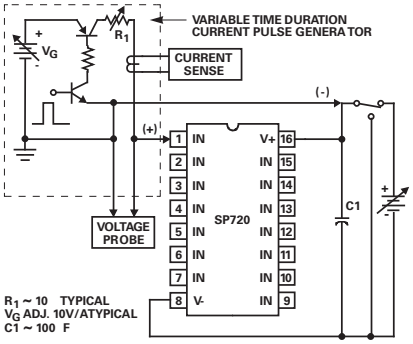
The test circuit of Figure 5 is shown with a positive pulse input. For a negative pulse input, the (-) current pulse input goes to an SP720 'IN' input pin and the (+) current pulse input goes to the SP720 V- pin. The V+ to V- supply of the SP720 must be allowed to float. (i.e., It is not tied to the ground reference of the current pulse generator.) Figure 6 shows the point of overstress as defined by increased leakage in excess of the data sheet published limits.

The maximum peak input current capability is dependent on the V+ to V- voltage supply level, improving as the supply voltage is reduced. Values of 0, 5, 15 and 30 voltages are shown. The safe operating range of the transient peak current should be limited to no more than 75% of the measured overstress level for any given pulse width as shown in Figure 6.

When adjacent input pins are paralleled, the sustained peak current capability is increased to nearly twice that of a single pin. For comparison, tests were run using dual pin combinations 1+2, 3+4, 5+6, 7+9, 10+11, 12+13 and 14+15.

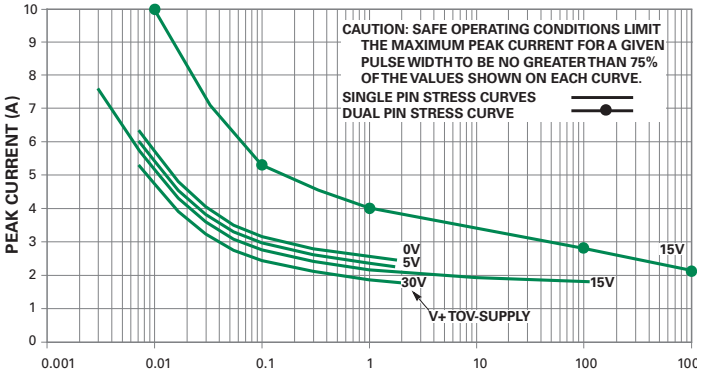
The overstress curve is shown in Figure 6 for a 15V supply condition. The dual pins are capable of 10A peak current for a 10µs pulse and 4A peak current for a 1ms pulse. The complete for single pulse peak current vs. pulse width time ranging up to 1 second are shown in Figure 6.

TYPICAL SP720 PEAK CURRENT TEST CIRCUIT WITH A VARIABLE PULSE WIDTH INPUT



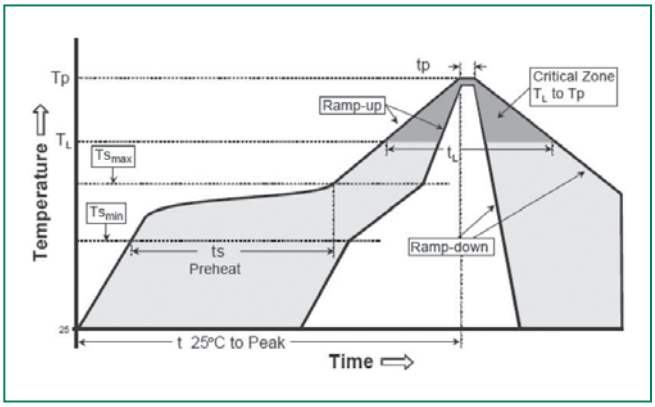
SP720 Typical Single Pulse Peak Current Curves

• Showing the Measured Point of Overstress in Amperes vs pulse width time in milliseconds (T_A = 25°C)

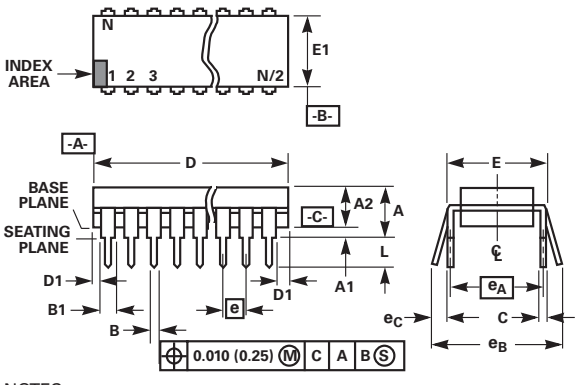


Soldering Parameters

Reflow Condition		Pb – Free assembly
Pre Heat	-Temperature Min ($T_{s(min)}$)	150°C
	-Temperature Max ($T_{s(max)}$)	200°C
	-Time (min to max) (t_s)	60 – 180 secs
Average ramp up rate (Liquidus) Temp (T_L) to peak		5°C/second max
$T_{S(max)}$ to T_L - Ramp-up Rate		5°C/second max
Reflow	-Temperature (T_L) (Liquidus)	217°C
	-Temperature (t_L)	60 – 150 seconds
Peak Temperature (T_P)		$250^{+0/-5}$ °C
Time within 5°C of actual peak Temperature (t_p)		20 – 40 seconds
Ramp-down Rate		5°C/second max
Time 25°C to peak Temperature (T_P)		8 minutes Max.
Do not exceed		260°C



Package Dimensions - Dual-In-Line Plastic Packages (PDIP)

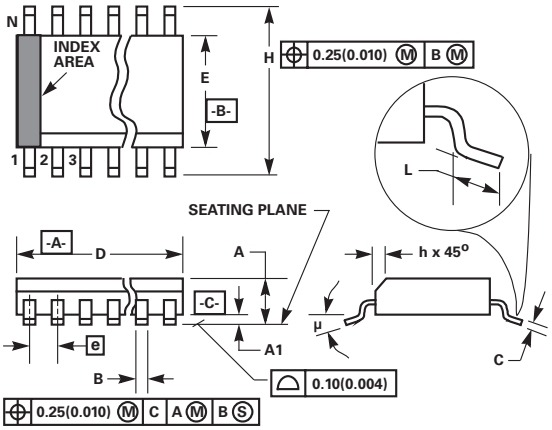


Package	PDIP				
Pins	16 Lead Dual-in-Line				
JEDEC	E16.3 MS-001-BB Issue D				
	Inches		Millimeters		Notes
	Min	Max	Min	Max	
A	-	0.21	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8, 10
C	0.008	0.014	0.204	0.355	-
D	0.735	0.775	18.66	19.68	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	16		16		9

Notes:

1. Controlling Dimensions: INCH. in case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JE-DEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

Package Dimensions - Small Outline Plastic Packages (SOIC)

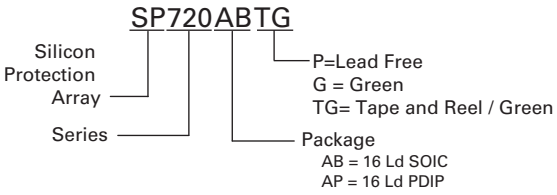


Package	SOIC				
Pins	16				
JEDEC	M16.15 (JEDEC MS-012-AC Issue C)				
	Inches		Millimeters		Notes
	Min	Max	Min	Max	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.3859	0.3937	9.80	10.00	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	16		16		7
μ	0°	8°	0°	8°	-

Notes:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension:MILLIMETER. Converted inch dimensions are not necessarily exact.

Part Numbering System



See Ordering Information section for specific options available

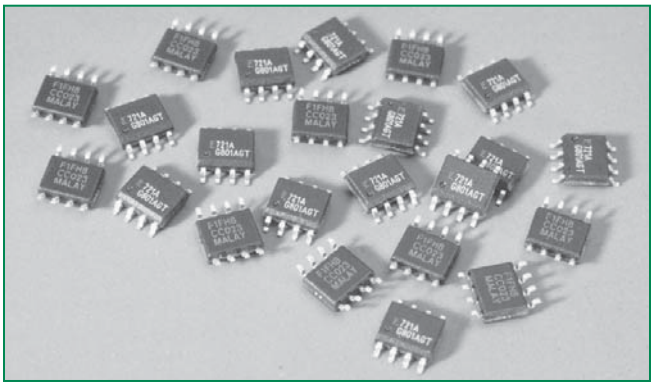
Product Characteristics

Lead Plating	Matte Tin
Lead Material	Copper Alloy
Lead Coplanarity	0.004 inches (0.102mm)
Subsitute Material	Silicon
Body Material	Molded Epoxy
Flammability	UL94-V-0

Ordering Information

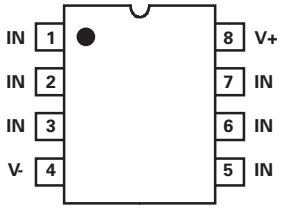
Part Number	Temp. Range (°C)	Package	Environmental Informaton	Marking	Min. Order
SP720APP	-40 to 105	16 Ld PDIP	Lead-free	720APP	1500
SP720ABG	-40 to 105	16 Ld SOIC	Green	720ABG	1920
SP720ABTG	-40 to 105	16 Ld SOIC Tape and Reel	Green	720ABG	2500

RoHS Pb SP721 Lead-Free/Green Series

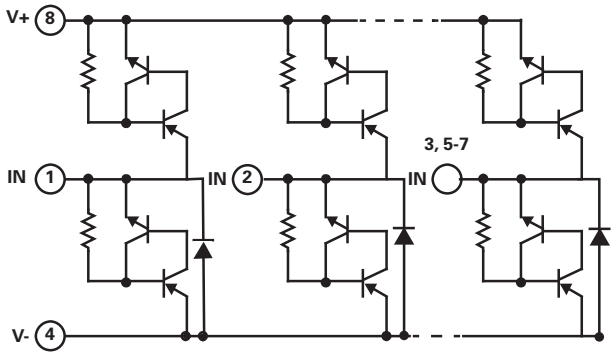


Pinout

SP721 (PDIP, SOIC)
TOP VIEW



Functional Block Diagram



Description

The SP721 is an array of SCR/Diode bipolar structures for ESD and over-voltage protection to sensitive input circuits. The SP721 has 2 protection SCR/Diode device structures per input. There are a total of 6 available inputs that can be used to protect up to 6 external signal or bus lines. Over-voltage protection is from the IN (Pins 1 - 3 and Pins 5 - 7) to V+ or V-.

The SCR structures are designed for fast triggering at a threshold of one $+V_{BE}$ diode threshold above V+ (Pin 8) or a $-V_{BE}$ diode threshold below V- (Pin 4). From an IN input, a clamp to V+ is activated if a transient pulse causes the input to be increased to a voltage level greater than one V_{BE} above V+. A similar clamp to V- is activated if a negative pulse, one V_{BE} less than V-, is applied to an IN input. Standard ESD Human Body Model (HBM) Capability is:

Features

- ESD Interface Capability for HBM Standards
  - MIL STD 3015.7 ..... 15kV
  - IEC 61000-4-2, Direct Discharge,
  - Single Input ..... 4kV (Level 2)
  - Two Inputs in Parallel ..... 8kV (Level 4)
  - IEC 61000-4-2, Air Discharge ..... 15kV (Level 4)
- High Peak Current Capability
  - IEC 61000-4-5 (8/20µs) ..... ±3A
  - Single Pulse, 100µs Pulse Width ..... ±2A
  - Single Pulse, 4µs Pulse Width ..... ±5A
- Designed to Provide Over-Voltage Protection
  - Single-Ended Voltage Range to ..... +30V
  - Differential Voltage Range to ..... ±15V
- Fast Switching ..... 2ns Rise Time
- Low Input Leakages ..... 1nA at 25°C Typical
- Low Input Capacitance ..... 3pF Typical
- An Array of 6 SCR/Diode Pairs
- Operating Temperature Range ..... -40°C to 105°C

Applications

- Microprocessor/Logic Input Protection
- Data Bus Protection
- Analog Device Input Protection
- Voltage Clamp

Absolute Maximum Ratings

Parameter	Rating	Units
Continuous Supply Voltage, (V+) - (V-)	+35	V
Forward Peak Current, I_{IN} to V_{CC}, I_{IN} to GND (Refer to Figure 6)	±2A, 100µs	V

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Note:
ESD Ratings and Capability (Figure 1, Table 1)
Load Dump and Reverse Battery (Note 2)

Thermal Information

Parameter	Rating	Units
Thermal Resistance (Typical, Note 1)	θ_{JA}	°C/W
PDIP Package	160	°C/W
SOIC Package	170	°C/W
Maximum Storage Temperature Range	-65 to 150	°C
Maximum Junction Temperature (Plastic Package)	150	°C
Maximum Lead Temperature (Soldering 10s) (SOIC Lead Tips Only)	300	°C

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Characteristics T_A = -40°C to 105°C, V_{IN} = 0.5V_{CC} , Unless Otherwise Specified

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Operating Voltage Range,	V_{SUPPLY}		-	2 to 30	-	V
V_{SUPPLY} = [(V+) - (V-)]						
Forward Voltage Drop						
IN to V-	V_{FWDL}	I_{IN} = 1A (Peak Pulse)	-	2	-	V
IN to V+	V_{FWDH}		-	2	-	V
Input Leakage Current	I_{IN}		-20	5	+20	nA
Quiescent Supply Current	$I_{QUIESCENT}$		-	50	200	nA
Equivalent SCR ON Threshold		Note 3	-	1.1	-	V
Equivalent SCR ON Resistance		V_{FWD}/I_{FWD}; Note 3	-	1	-	W
Input Capacitance	C_{IN}		-	3	-	pF
Input Switching Speed	t_{ON}		-	2	-	ns

Notes:

2. In automotive and battery operated systems, the power supply lines should be externally protected for load dump and reverse battery. When the V+ and V- Pins are connected to het same supply voltage source as the device or control line under protection, a current limiti ng resistor should be connected in series between the external supply and the SP721 supply pins to limit reverse battery current to within the rated maximum limits. Bypass capacitors of typically 0.01µF or larger romf the V+ and V- Pins to ground are recommended.
3. Refer to the Figure 3 graph for definitions of equivalent "SCR ON Threshold" and "SCR ON Resistance". These characteristics are given here for thumb-rule nformation to determine peak current and dissipation under EOS conditions.

ESD Capability

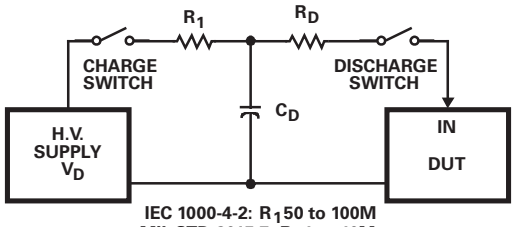
ESD capability is dependent on the application and defined test standard.The evaluation results for various test standards and methods based on Figure 1 are shown in Table 1.

For the "Modified"MIL-STD-3015.7 condition that is defined as an "in-circuit" method of ESD testing, the V+ and V- pins have a return path to ground and the SP721 ESD capability is typically greater than 15kV from 100pF through 1.5kΩ.By strict definition of MIL-STD-3015.7 using "pin-to-pin"device testing, the ESD voltage capability is greater than 6kV.The MIL-STD-3015.7 results were determined from AT&T ESD Test Lab measurements.

The HBM capability to the IEC 61000-4-2 standard is greater than 15kV for air discharge (Level 4) and greater than 4kV for direct discharge (Level 2).Dual pin capability (2 adjacent pins in parallel) is well in excess of 8kV (Level 4).

For ESD testing of the SP721 to EIAJ IC121 Machine Model (MM) standard, the results are typically better than 1kV from 200pF with no series resistance.

ELECTROSTATIC DISCHARGE TEST

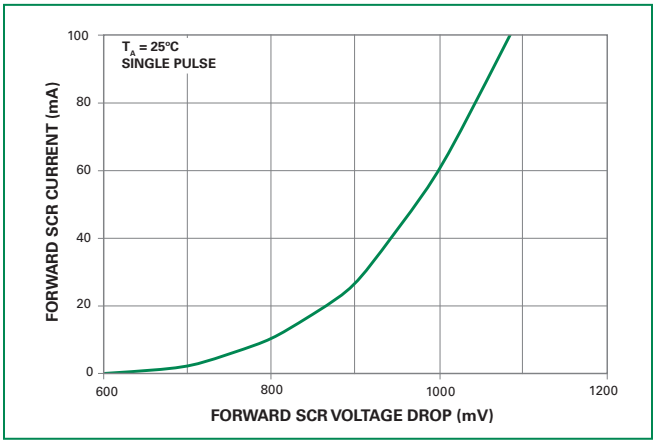


IEC 1000-4-2: R_1 50 to 100M
MIL-STD-3015.7: R_1 1 to 10M

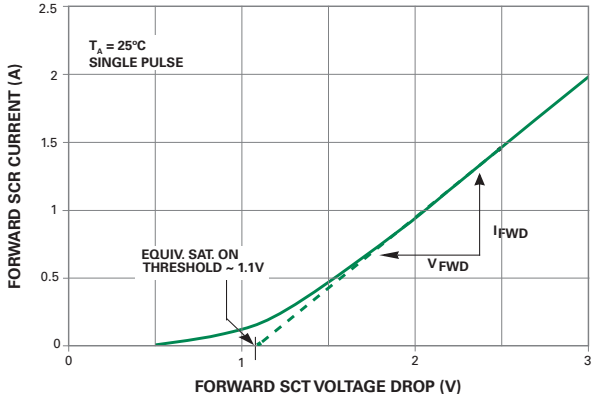
ESD Test Conditions

STANDARD	TYPE/MODE	R_D	C_D	$\pm V_D$
MIL STD 3015.7	Modified HBM	1.5kΩ	100pF	15kV
	Standard HBM	1.5kΩ	100pF	6kV
IEC 61000-4-2	HBM, Air Discharge	330Ω	150pF	15kV
	HBM, Direct Discharge	330Ω	150pF	4kV
	HBM, Direct Discharge, Two Parallel Input Pins	330Ω	150pF	8kV
EIAJ IC121	Machine Model	0kΩ	200pF	1kV

Low Current SCR Forward Voltage Drop Curve



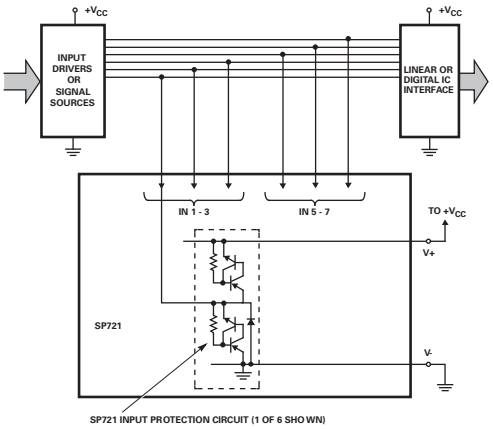
High Current SCR Forward Voltage Drop Curve



Lead-Free/Green SP721

Typical Application of the SP721

• (Application as an Input Clamp for Over-voltage, Greater than 1V_{BE} Above V+ or less than -1V_{BE} below V-)



Peak Transient Current Capability of the SP721

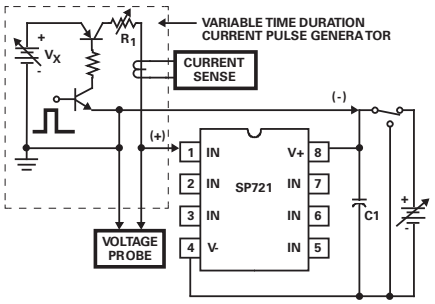
The peak transient current capability rises sharply as the width of the current pulse narrows. Destructive testing was done to fully evaluate the SP721's ability to withstand a wide range of peak current pulses vs time. The circuit used to generate current pulses is shown in Figure 5.

The test circuit of Figure 5 is shown with a positive pulse input. For a negative pulse input, the (-) current pulse input goes to an SP721 'IN' input pin and the (+) current pulse input goes to the SP721 V- pin. The V+ to V- supply of the SP721 must be allowed to float. (i.e., It is not tied to the ground reference of the current pulse generator.) Figure 6 shows the point of overstress as defined by increased leakage in excess of the data sheet published limits.

The maximum peak input current capability is dependent on the ambient temperature, improving as the temperature is reduced. Peak current curves are shown for ambient temperatures of 25ºC and 105ºC and a 15V power supply condition. The safe operating range of the transient peak current should be limited to no more than 75% of the measured overstress level for any given pulse width as shown in the curves of Figure 6.

Note that adjacent input pins of the SP721 may be paralleled to improve current (and ESD) capability. The sustained peak current capability is increased to nearly twice that of a single pin.

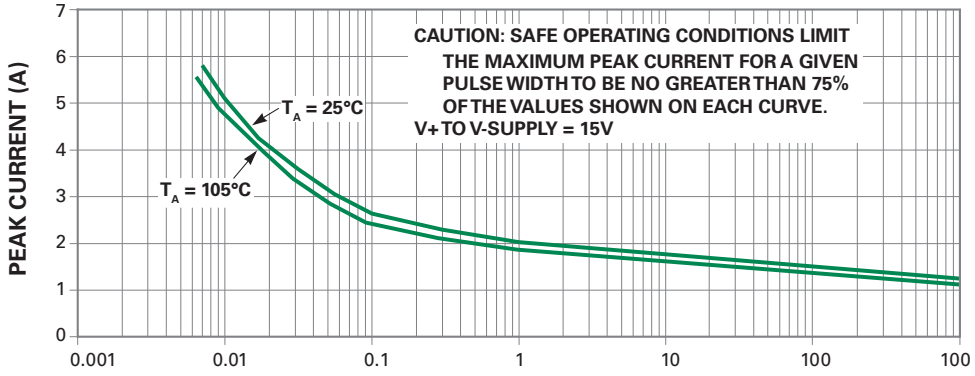
TYPICAL SP721 PEAK CURRENT TEST CIRCUIT WITH A VARIABLEPULSE WIDTH INPUT



R_1 ~ 10 TYPICAL
V_X ADJ. 10V/ATYPICAL
C1 ~ 100 F

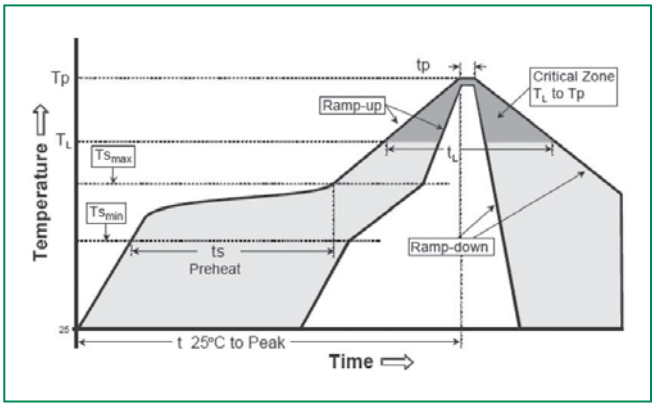
SP721 Typical Single Pulse Peak Current Curves

• Showing the Measured Point of Overstress in Amperes vs pulse width time in milliseconds

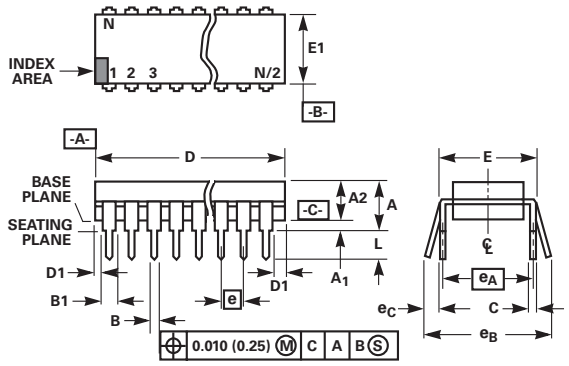


Soldering Parameters

Reflow Condition		Pb – Free assembly
Pre Heat	-Temperature Min ($T_{s(min)}$)	150°C
	-Temperature Max ($T_{s(max)}$)	200°C
	-Time (min to max) (t_s)	60 – 180 secs
Average ramp up rate (Liquidus) Temp (T_L) to peak		5°C/second max
$T_{S(max)}$ to T_L - Ramp-up Rate		5°C/second max
Reflow	-Temperature (T_L) (Liquidus)	217°C
	-Temperature (t_L)	60 – 150 seconds
Peak Temperature (T_P)		$250^{+0/-5}$ °C
Time within 5°C of actual peak Temperature (t_p)		20 – 40 seconds
Ramp-down Rate		5°C/second max
Time 25°C to peak Temperature (T_P)		8 minutes Max.
Do not exceed		260°C



Package Dimensions - Dual-In-Line Plastic Packages (PDIP)

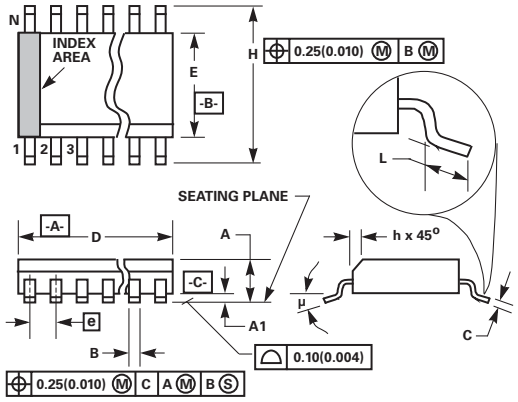


Notes:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C- .
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is t he maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

Package	PDIP				
Pins	8 Lead Dual-in-Line				
JEDEC	E8.3 MS-001-BA Issue D				
	Inches		Millimeters		Notes
	Min	Max	Min	Max	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8, 10
C	0.008	0.014	0.204	0.355	-
D	0.355	0.400	9.01	10.16	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	8		8		9

Package Dimensions - Small Outline Plastic Packages (SOIC)

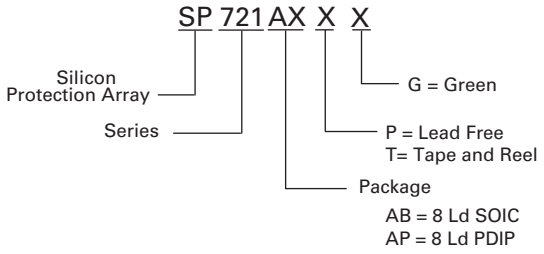


Package	SOIC				
Pins	8				
JEDEC	M8.15 (JEDEC MS-012-AA Issue C)				
	Inches		Millimeters		Notes
	Min	Max	Min	Max	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.1890	0.1968	4.80	5.00	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	8		8		7
μ	0°	8°	0°	8°	-

Notes:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Inter-lead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

Part Numbering System



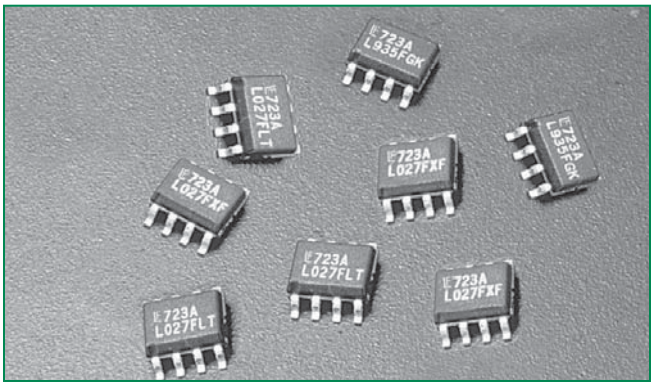
Product Characteristics

Lead Plating	Matte Tin
Lead Material	Copper Alloy
Lead Coplanarity	0.004 inches (0.102mm)
Subsitute Material	Silicon
Body Material	Molded Epoxy
Flammability	UL94-V-0

Ordering Information

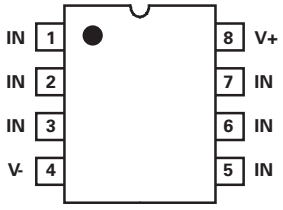
Part Number	Temp. Range (°C)	Package	Environmental Informaton	Marking	Min. Order
SP721APP	-40 to 105	8 Ld PDIP	Lead-free	721APP	2000
SP721ABG	-40 to 105	8 Ld SOIC	Green	721AG	1960
SP721ABTG	-40 to 105	8 Ld SOIC Tape and Reel	Green	721AG	2500

RoHS Pb GREEN SP723 Lead-Free/Green Series

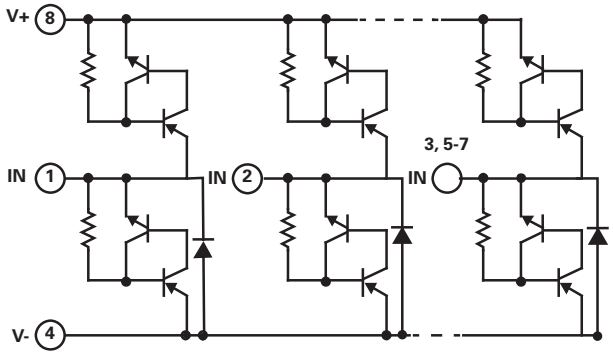


Pinout

SP723 (PDIP, SOIC)
TOP VIEW



Functional Block Diagram



Description

The SP723 is an array of SCR/Diode bipolar structures for ESD and over-voltage protection of sensitive input circuits. The SP723 has 2 protection SCR/Diode device structures per input. There are a total of 6 available inputs that can be used to protect up to 6 external signal or bus lines. Over-voltage protection is from the IN (Pins 1 - 3 and Pins 5 - 7) to V+ or V-.

The SCR structures are designed for fast triggering at a threshold of one $+V_{BE}$ diode threshold above V+ (Pin 8) or a $-V_{BE}$ diode threshold below V- (Pin 4). From an IN input, a clamp to V+ is activated if a transient pulse causes the input to be increased to a voltage level greater than one V_{BE} above V+. A similar clamp to V- is activated if a negative pulse, one V_{BE} less than V-, is applied to an IN input.

Refer to Fig 1 and Table 1 for further details. Refer to Application Note AN9304 and AN9612 for further detail.

Features

- ESD Interface per HBM Standards
  - IEC 61000-4-2, Direct Discharge ..... 8kV (Level 4)
  - IEC 61000-4-2, Air Discharge.....15kV (Level 4)
  - MIL-STD-3015.7 .....25kV
- Peak Current Capability
  - IEC 61000-4-5 8/20µs Peak Pulse Current..... ±7A
  - Single Transient Pulse, 100s Pulse Width ..... ±4A
- Designed to Provide Over-Voltage Protection
  - Single-Ended Voltage Range to ..... +30V
  - Differential Voltage Range to ..... ±15V
- Fast Switching.....2ns Risetime
- Low Input Leakages.....2nA at 25°C Typical
- Low Input Capacitance.....5pF Typical
- An Array of 6 SCR/Diode Pairs
- Operating Temperature Range.....-40°C to 105°C

Applications

- Microprocessor/Logic Input Protection
- Data Bus Protection
- Analog Device Input Protection
- Voltage Clamp

Absolute Maximum Ratings

Parameter	Rating	Units
Continuous Supply Voltage, (V+) - (V-)	+35	V
Forward Peak Current, I_{IN} to V_{CC}, I_{IN} to GND (Refer to Figure 6)	±4A, 100µs	V
Peak Pulse Current, 8/20µs	±7A	V

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Note:
ESD Ratings and Capability (Figure 1, Table 1)
Load Dump and Reverse Battery (Note 2)

Thermal Information

Parameter	Rating	Units
Thermal Resistance (Typical, Note 1)	θ_{JA}	°C/W
PDIP Package	160	°C/W
SOIC Package	170	°C/W
Storage Temperature Range	-65 to 150	°C
Maximum Junction Temperature (Plastic Package)	150	°C
Lead Temperature (Soldering 10s) (SOIC Lead Tips Only)	300	°C

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Characteristics T_A = -40°C to 105°C, V_{IN} = 0.5V_{CC} , Unless Otherwise Specified

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Operating Voltage Range, V_{SUPPLY} =[(V+)-(V-)]	V_{SUPPLY}		-	2 to 30	-	V
Forward Voltage Drop						
IN to V-	V_{FWDL}	I_{IN}=2A(Peak Pulse)	-	2	-	V
IN to V+	V_{FWDH}		-	2	-	V
Input Leakage Current	I_{IN}		-20	5	20	nA
Quiescent Supply Current	$I_{QUIESCENT}$		-	50	200	nA
Equivalent SCR ON Threshod		Note 3	-	1.1	-	V
Equivalent SCR ON Resistance		V_{FWD}/I_{FWD}; Note 3	-	0.5	-	Ω
Input Capacitance	C_{IN}		-	5	-	PF
Input Switching Speed	t_{ON}		-	2	-	ns

Notes:

2. In automotive ans battery operated systems, the power supply lines should be externally protected for load dump and reverse battery. When the V+ and V- Pins are connected to the same supply voltage source as the device or control line under protection, acurrent limiting resistor should be connectied in series between the external supply and the SP723 supply pins to limit reverse battery current to within the rated maximum limits. Bypass capacitors of typically 0.01µF or larger from the V+ and V- Pins to ground are recommended.
3. Refer to the Figure 3 graph for determine peak current and dessipation under EOS conditions.

ESD Capability

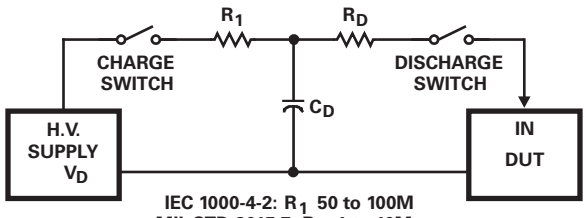
ESD capability is dependent on the application and defined test standard.The evaluation results for various test standards and methods based on Figure 1 are shown in Table 1.

The SP723 has a Level 4 HBM capability when tested as a device to the IEC 61000-4-2 standard. Level 4 specifies a required capability greater than 8kV for direct discharge and greater than 15kV for air discharge.

For the "Modified" MIL-STD-3015.7 condition that is defined as an "in-circuit" method of ESD testing, the V+ and V- pins have a return path to ground and the SP723 ESD capability is typically greater than 25kV from 100pF through 1.5kΩ. By strict definition of MIL-STD-3015.7 using "pin-to-pin" device testing, the ESD voltage capability is greater than 10kV.

For the SP723 EIAJ IC121 Machine Model (MM) standard, the ESD capability is typically greater than 2kV from 200pF with no series resistance.

ELECTROSTATIC DISCHARGE TEST

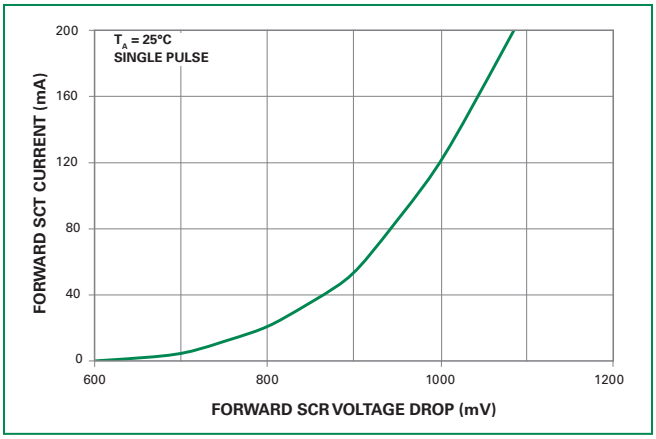


IEC 1000-4-2: R_1 50 to 100M
MIL-STD-3015.7: R_1 1 to 10M

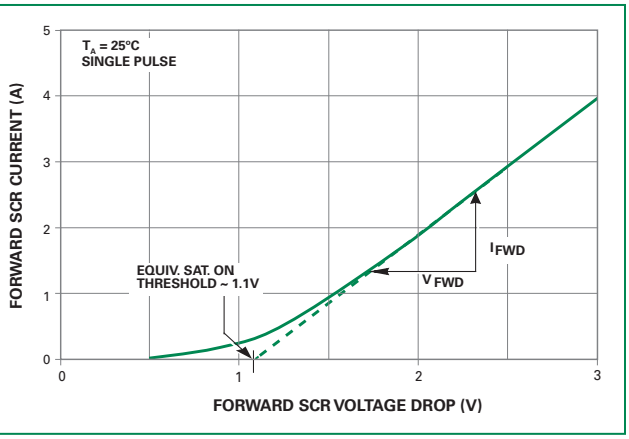
ESD Test Conditions

STANDARD	TYPE/MODE	R_D	C_D	$\pm V_D$
IEC 1000-4-2 (Level 4)	HBM, Air Discharge	330 Ω	150pF	15kV
	HBM, Direct Discharge	330 Ω	150pF	8kV
MIL-STD-3015.7	Modified HBM	1.5k Ω	100pF	25kV
	Standard HBM	1.5k Ω	100pF	10kV
EIAJ IC121	Machine Model	0k Ω	200pF	2kV
EIAJ IC121	Machine Model	0kΩ	200pF	1kV

Low Current SCR Forward Voltage Drop Curve



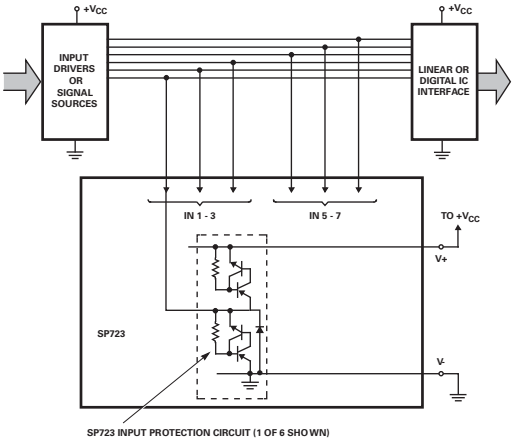
High Current SCR Forward Voltage Drop Curve



Lead-Free/Green SP723

Typical Application of the SP723

• (Application as an Input Clamp for Over-voltage, Greater than 1V_{BE} Above V+ or less than -1V_{BE} below V-)



Peak Transient Current Capability of the SP723

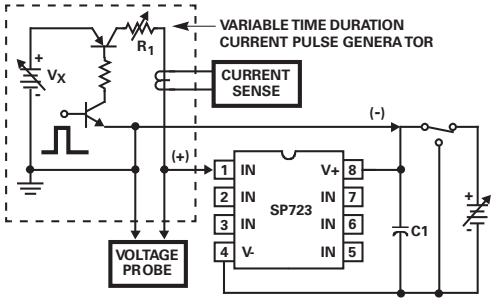
The peak transient current capability rises sharply as the width of the current pulse narrows. Destructive testing was done to fully evaluate the SP723's ability to withstand a wide range of peak current pulses vs time. The circuit used to generate current pulses is shown in Figure 5.

The test circuit of Figure 5 is shown with a positive pulse input. For a negative pulse input, the (-) current pulse input goes to an SP723 'IN' input pin and the (+) current pulse input goes to the SP723 V- pin. The V+ to V- supply of the SP723 must be allowed to float. (i.e., It is not tied to the ground reference of the current pulse generator.) Figure 6 shows the point of overstress as defined by increased leakage in excess of the data sheet published limits.

The maximum peak input current capability is dependent on the ambient temperature, improving as the temperature is reduced. Peak current curves are shown for ambient temperatures of 25ºC and 105ºC and a 15V power supply condition. The safe operating range of the transient peak current should be limited to no more than 75% of the measured overstress level for any given pulse width as shown in the curves of Figure 6.

Note that adjacent input pins of the SP723 may be paralleled to improve current (and ESD) capability. The sustained peak current capability is increased to nearly twice that of a single pin.

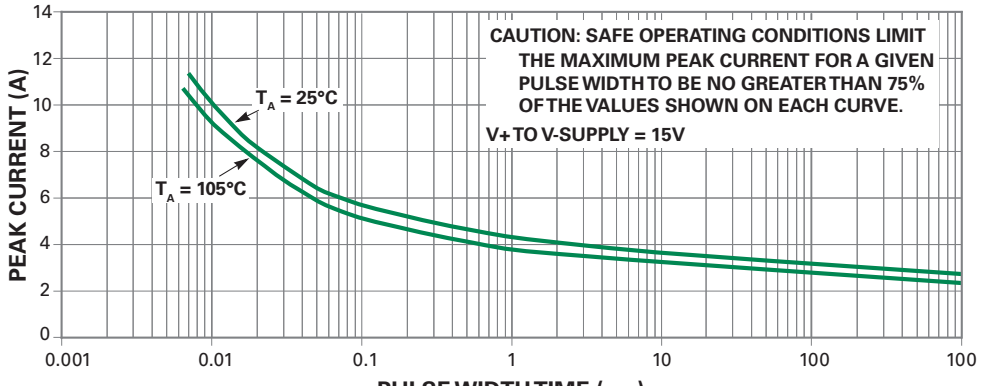
TYPICAL SP723 PEAK CURRENT TEST CIRCUIT WITH A VARIABLEPULSE WIDTH INPUT



R_1 ~ 10 TYPICAL
V_X ADJ. 10V/ATYPICAL
C1 ~ 100 F

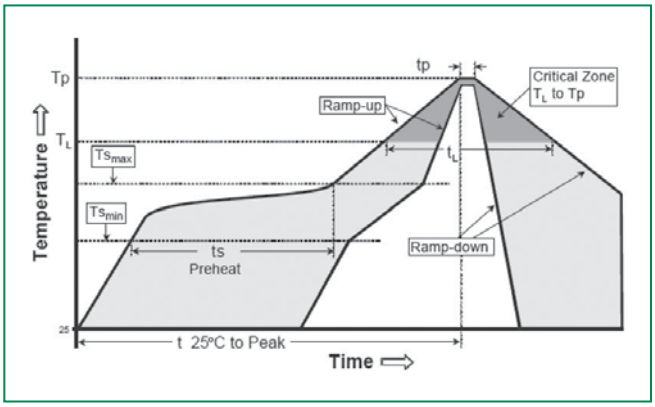
SP723 Typical Single Pulse Peak Current Curves

• Showing the Measured Point of Overstress in Amperes vs pulse width time in milliseconds

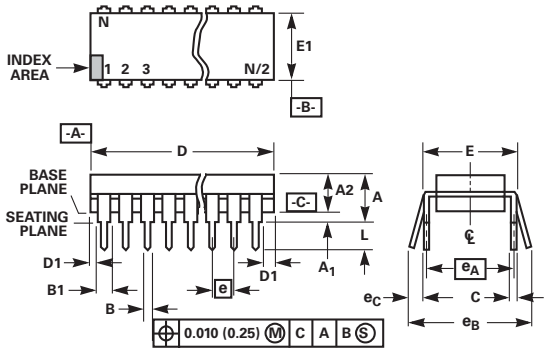


Soldering Parameters

Reflow Condition		Pb – Free assembly
Pre Heat	-Temperature Min ($T_{s(min)}$)	150°C
	-Temperature Max ($T_{s(max)}$)	200°C
	-Time (min to max) (t_s)	60 – 180 secs
Average ramp up rate (Liquidus) Temp (T_L) to peak		5°C/second max
$T_{S(max)}$ to T_L - Ramp-up Rate		5°C/second max
Reflow	-Temperature (T_L) (Liquidus)	217°C
	-Temperature (t_L)	60 – 150 seconds
Peak Temperature (T_P)		$250^{+0/-5}$ °C
Time within 5°C of actual peak Temperature (t_p)		20 – 40 seconds
Ramp-down Rate		5°C/second max
Time 25°C to peak Temperature (T_P)		8 minutes Max.
Do not exceed		260°C



Package Dimensions - Dual-In-Line Plastic Packages (PDIP)

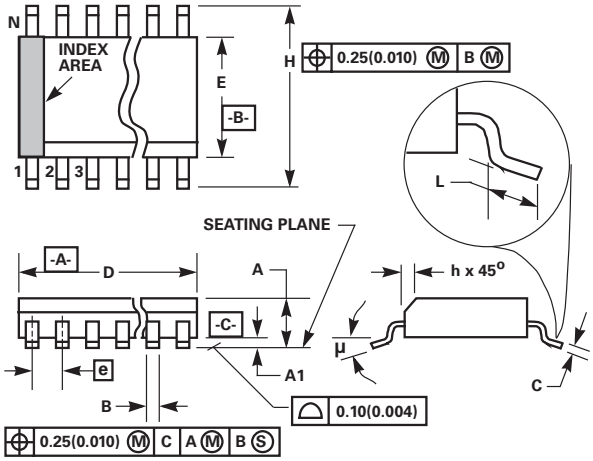


Notes:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads unconstrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads uncon-strained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

Package	PDIP				
Pins	8				
JEDEC	E8.3 (JEDEC MS-001-BA Issue D)				
	Inches		Millimeters		Notes
	Min	Max	Min	Max	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8, 10
C	0.008	0.014	0.204	0.355	-
D	0.355	0.400	9.01	10.16	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.1	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	8		8		9

Package Dimensions - Small Outline Plastic Packages (SOIC)

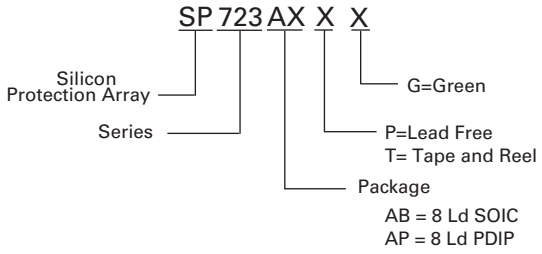


Package	SOIC				
Pins	8				
JEDEC	M8.15 (JEDEC MS-012-AA Issue C)				
	Inches		Millimeters		Notes
	Min	Max	Min	Max	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.1890	0.1968	4.80	5.00	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	8		8		7
μ	0°	8°	0°	8°	-

Notes:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Inter-lead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The eadl width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension:MILLIMETER. Converted inch dimensions are not necessarily exact.

Part Numbering System



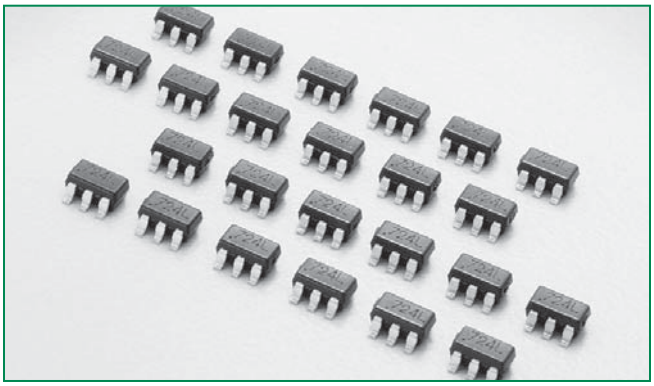
Product Characteristics

Lead Plating	Matte Tin
Lead Material	Copper Alloy
Lead Coplanarity	0.004 inches (0.102mm)
Subsitute Material	Silicon
Body Material	Molded Epoxy
Flammability	UL94-V-0

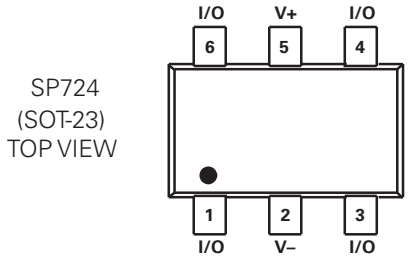
Ordering Information

Part Number	Temp. Range (°C)	Package	Environmental Informaton	Marking	Min. Order
SP723APP	-40 to 105	8 Ld PDIP	Lead-free	723APP	2000
SP723ABG	-40 to 105	8 Ld SOIC	Green	723AG	1960
SP723ABTG	-40 to 105	8 Ld SOIC Tape and Reel	Green	723AG	2500

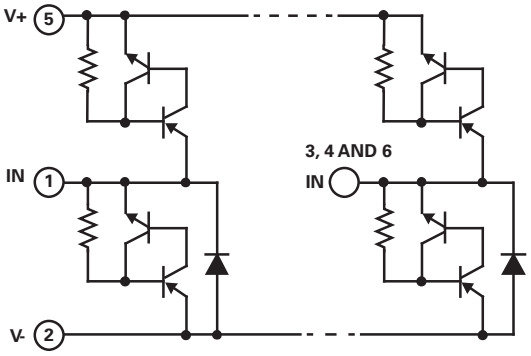
RoHS Pb SP724 Lead-Free/Green Series



Pinout



Functional Block Diagram



Notes:

1. The design of the SP724 SCR/Diode ESD Protection Arrays are covered by Littelfuse patent 4567500.
2. The full ESD capability of the SP724 is achieved when wired in a circuit that includes connection to both the V+ and V- pins. When handling individual devices, follow proper procedures for electrostatic discharge.

Description

The SP724 is a quad array of transient voltage clamping circuits designed to suppress ESD and other transient over-voltage events. The SP724 is used to help protect sensitive digital or analog input circuits on data, signal, or control lines operating on power supplies up to 20VDC.

The SP724 is comprised of bipolar SCR/diode structures to protect up to four independent lines by clamping transients of either polarity to the power supply rails. The SP724 offers very low leakage (1nA Typical) and low input capacitance (3pF Typical). Additionally, the SP724 is rated to withstand the IEC 61000-4-2 ESD specification for both contact and air discharge methods to level 4.

The SP724 is connected to the sensitive input line and its associated power supply lines. Clamping action occurs during the transient pulse, turning on the diode and fast triggering SCR structures when the voltage on the input line exceeds one V_{BE} threshold above the V+ supply (or one V_{BE} threshold below the V- supply). Therefore, the SP724P operation is unaffected by poor power supply regulation or voltage fluctuations within its operating range.

Features

- An Array of 4 SCR/Diode Pairs in 6-Lead SOT-23
- ESD Capability per HBM Standards
  - IEC 61000-4-2, Direct Discharge ..... 8kV (Level 4)
  - IEC 61000-4-2, Air Discharge.....15kV (Level 4)
  - MIL STD 3015.7..... >8kV
- Input Protection for Applications with Power Supplies Up to +20V (Single-Ended Voltage), and ±10V (Differential Voltage)
- Peak Current Capability
  - IEC 61000-4-5 (8/20µs) ..... ±3A
  - Single Pulse, 100µs Pulse Width ..... ±2.2A
- Low Input Leakage..... 1nA Typical
- Low Input Capacitance.....3pF Typical
- Operating Temperature Range.....-40°C to 105°C

Applications

- Microprocessor/Logic Input Protection
- Data Bus Protection
- Analog Device Input Protection
- Voltage Clamp

Absolute Maximum Ratings

Parameter	Rating	Units
Continuous Supply Voltage, (V+) - (V-)	+20	V
Forward Peak Current, I_{IN} to V_{CC} , GND (Refer to Figure 6)	±2.2A, 100µs	V

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Note :

ESD Ratings and Capability - See Figure 1, Table 1

Thermal Information

Parameter	Rating	Units
Thermal Resistance (Typical, Note 3)	θ_{JA}	°C/W
SOT Package	220	°C/W
Maximum Storage Temperature Range	-65 to 150	°C
Maximum Junction Temperature	150	°C
Maximum Lead Temperature (Soldering 10s) (SOT - Lead Tips Only)	300	°C

Note: 3. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Characteristics T_A = -40°C to 105°C, V_{IN} = 0.5V_{CC} , Unless Otherwise Specified

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Operating Voltage Range, V_{SUPPLY} = [(V+) - (V-)] (Notes 4, 5)	V_{SUPPLY}		1	-	20	V
Forward Voltage Drop						
Forward Voltage Drop IN to V-	V_{FWDL}	I_{IN} = 1A (Peak Pulse)	-	2	-	V
IN to V+	V_{FWDH}		-	2	-	V
Input Leakage Current	I_{IN}		-10	1	10	nA
Quiescent Supply Current	$I_{QUIESCENT}$	V+ = 20V, V- = GND	-	-	100	nA
Equivalent SCR ON Threshold		(Note 6)	-	1.1	-	V
Equivalent SCR ON Resistance		V_{FWD}/I_{FWD} (Note 6)	-	1.0	-	Ω
Input Capacitance	C_{IN}		-	3	-	pF

Notes:

4. In automotive and other battery charging systems, the SP724 power supply lines should be externally protected for load dump and reverse battery. When the V+ and V- Pins are connected to the same supply voltage source as the device or control line under protection, a current limiting resistor should be connected in series between the external supply and the SP724 supply pins to limit reverse battery current to within the rated maximum limits.
5. Bypass capacitors of typically 0.01µF or larger should be connected closely between the V+ and V- Pins for all applications.
6. Refer to the Figure 3 graph for definitions of equivalent "SCR ON Threshold" and "SCR ON Resistance". These characteristics are given here for information to determine peak current and dissipation under EOS conditions.

ESD Capability

ESD rating is dependent on the defined test standard. The evaluation results for various test standards and methods based on Figure 1 are shown in Table 1.3

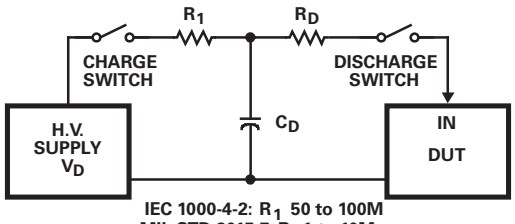
The SP724 has a Level 4 rating when tested to the IEC 61000-4-2 Human Body Model (HBM) standard and connected in a circuit in which the V+ and V- pins have a return path to ground. Level 4 specifies a required capability greater than 8kV for direct discharge and greater than 15kV for air discharge.

The "Modified" MIL-STD-3015.7 condition is defined as an "in-circuit" method of ESD testing, the V+ and V- pins have a return path to ground.The SP724 ESD capability is greater than 8kV with 100pF discharged through 1.5kΩ. By strict definition of the standard MIL-STD-3015.7 method using "pin-to-pin" device testing, the ESD voltage capability is greater than 2kV.

For the SP724 EIAJ IC121 Machine Model (MM) standard, the ESD capability is typically greater than 1.8kV with 200pF discharged through 0kΩ.

The Charged Device model is based upon the self-capacitance of the SOT-23 package through 0kΩ.

ELECTROSTATIC DISCHARGE TEST



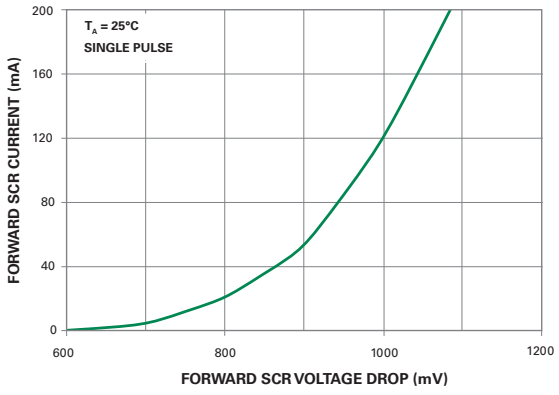
IEC 1000-4-2: R_1 50 to 100M
MIL STD 3015.7: R_1 1 to 10M

ESD Test Conditions

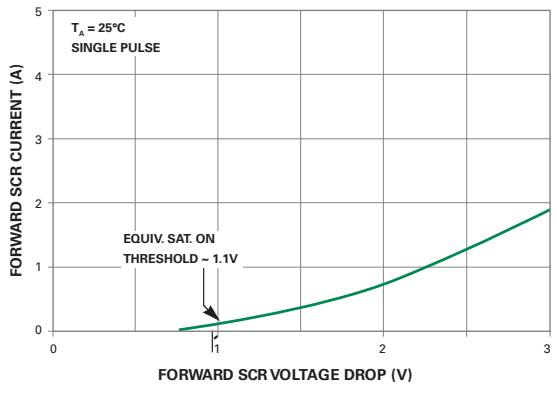
STANDARD	TYPE/MODE	R_D	C_D	$\pm V_D$
IEC 61000-4-2 (Level 4)	HBM, Air Discharge	330 Ω	150pF	15kV
	HBM, Direct Discharge	330 Ω	150pF	8kV
MIL-STD-3015.7	Modified HBM	1.5k Ω	100pF	8kV †
	Standard HBM	1.5k Ω	100pF	2kV
EIAJ IC121	Machine Model	0k Ω	200pF	400V
US ESD DS 5.3	Charged Device Model	0k Ω	NA	3kV

†Upper limit of laboratory test set.

Low Current SCR Forward Voltage Drop Curve



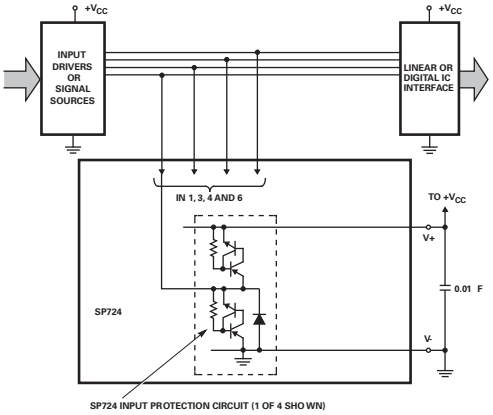
High Current SCR Forward Voltage Drop Curve



Lead-Free/Green SP724

Typical Application of the SP724

• (Application as an Input Clamp for Over-voltage, Greater than $1V_{BE}$ Above V+ or less than $-1V_{BE}$ below V-)



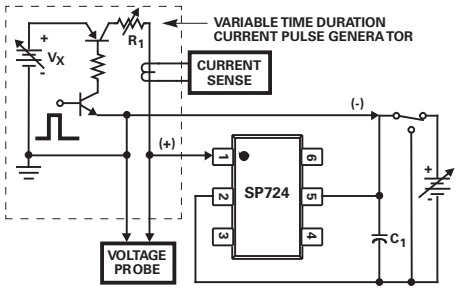
Peak Transient Current Capability for Long Duration Surges

The peak transient current capability is inversely proportional to the width of the current pulse. Testing was done to fully evaluate the SP724's ability to withstand long duration current pulses using the circuit of Figure 5. Figure 6 shows the point of overstress as defined by increased leakage in excess of the data sheet published limits. The safe operating range of the transient peak current should be limited to no more than 75% of the measured overstress level for any given pulse width as shown in the curve of Figure 6.

The test circuit of Figure 5 is shown with a positive pulse input. For a negative pulse input, the (-) current pulse input goes to an SP724 'IN' input pin and the (+) current pulse input goes to the SP724 V- pin. The V+ to V- supply of the SP724 must be allowed to float. (i.e., It is not tied to the ground reference of the current pulse generator.)

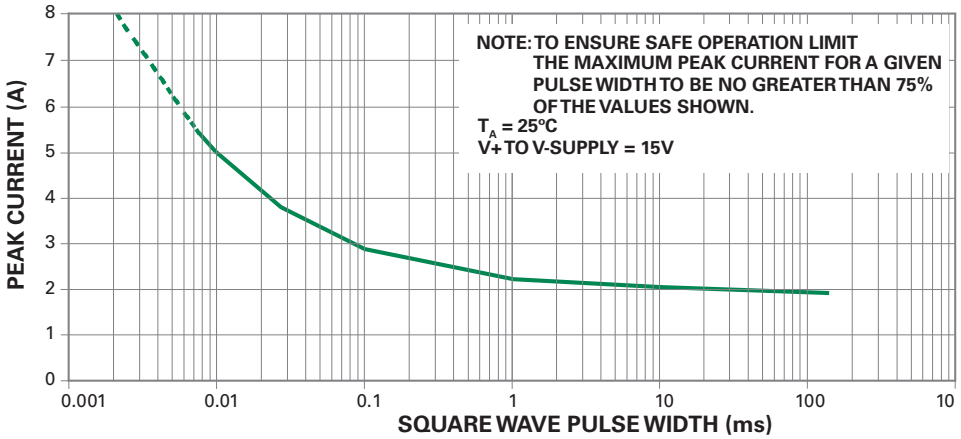
Note that two input pins of the SP724 may be paralleled to improve current (and ESD) capability. The sustained peak current capability is increased to nearly twice that of a single pin.

TYPICAL SP724 PEAK CURRENT TEST CIRCUIT WITH A VARIABLE PULSE WIDTH INPUT



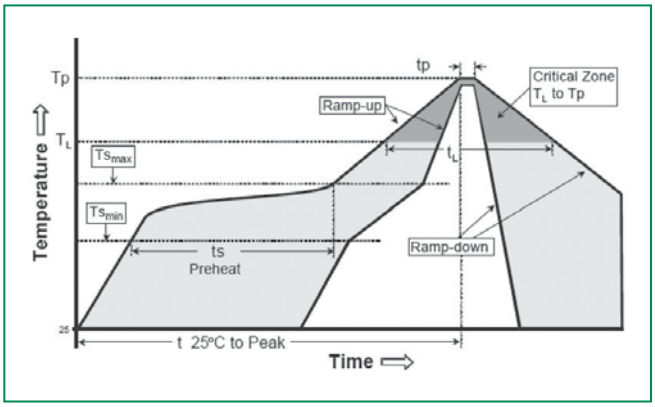
SP724 Typical Nonrepetitive Peak Current Pulse Capability

• Showing the Measured Point of Overstress in Amperes vs pulse width time in milliseconds

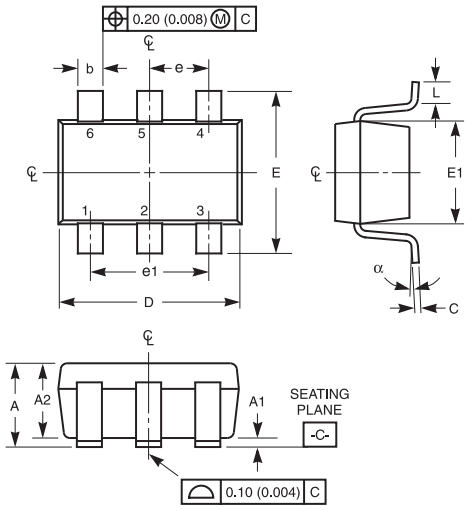


Soldering Parameters

Reflow Condition		Pb – Free assembly
Pre Heat	-Temperature Min ($T_{s(min)}$)	150°C
	-Temperature Max ($T_{s(max)}$)	200°C
	-Time (min to max) (t_s)	60 – 180 secs
Average ramp up rate (Liquidus) Temp (T_L) to peak		5°C/second max
$T_{S(max)}$ to T_L - Ramp-up Rate		5°C/second max
Reflow	-Temperature (T_L) (Liquidus)	217°C
	-Temperature (t_L)	60 – 150 seconds
Peak Temperature (T_P)		$250^{+0/-5}$ °C
Time within 5°C of actual peak Temperature (t_p)		20 – 40 seconds
Ramp-down Rate		5°C/second max
Time 25°C to peak Temperature (T_P)		8 minutes Max.
Do not exceed		260°C



Package Dimensions - Small Outline Transistor Plastic Packages (SOT23-6)

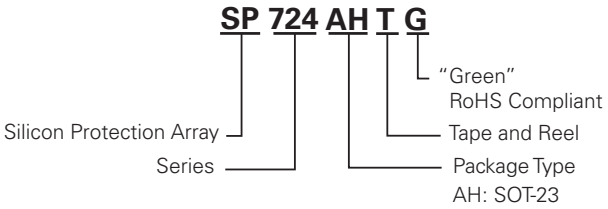


Package	SOT23-6				
Pins	6				
JEDEC	MO-203 Issue A				
	Inches		Millimeters		Notes
	Min	Max	Min	Max	
A	0.036	0.057	0.9	1.45	-
A1	0.000	0.0059	0	0.15	-
A2	0.036	0.051	0.9	1.30	-
b	0.0138	0.0196	0.35	0.50	-
C	0.0036	0.0078	0.09	0.20	-
D	0.111	0.118	2.8	3.00	3
E	0.103	0.118	2.6	3.00	-
E1	0.060	0.068	1.5	1.75	3
e	0.0374 Ref		0.95 Ref		-
e1	0.0748 Ref		1.9 Ref		-
L	0.004	0.023	0.10	0.60	4, 5
N	6		6		6
α	0°	10°	0°	10°	-

Notes:

1. Dimensioning and tolerances per ANSI 14.5M-1982.
2. Package conforms to EIAJ SC-74 (1992).
3. Dimensions D and E1 are exclusive of mold flash, protrusions, or gate burrs.
4. Footlenth L measured at reference to seating plane.
5. "L" is the length of flat foot surface for soldering to substrate.
6. "N" is the number of terminal positions.
7. Controling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

Part Numbering System



Product Characteristics

Lead Plating	Matte Tin
Lead Material	Copper Alloy
Lead Coplanarity	0.004 inches (0.102mm)
Subsitute Material	Silicon
Body Material	Molded Epoxy
Flammability	UL94-V-0

Notes:

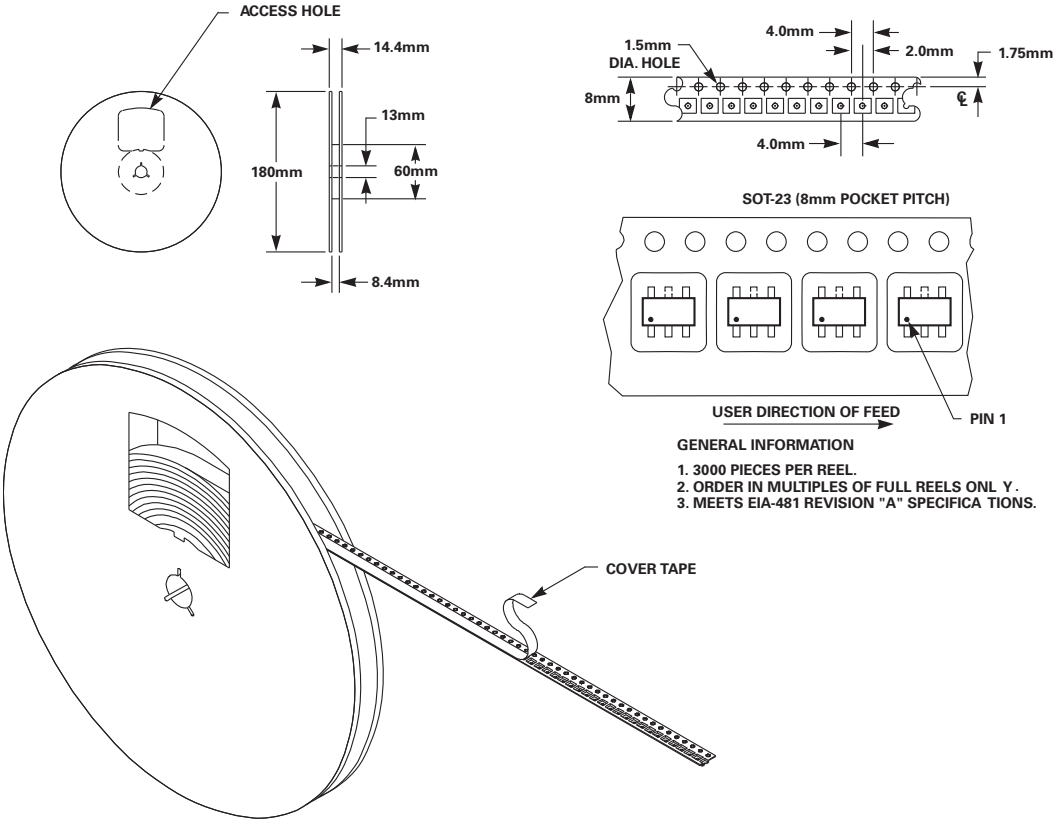
1. All dimensions are in millimeters.
2. Dimensions include solder plating.
3. Dimensions are exclusive of mold flash & metal burr.
4. All specifications comply to JEDEC SPEC MO-203 ISSUE A.
5. Blo is facing up for mold and facing down for trim/form, i.e. reverse trim/form.
6. Package surface matte finish VDI 11-13.

Ordering Information

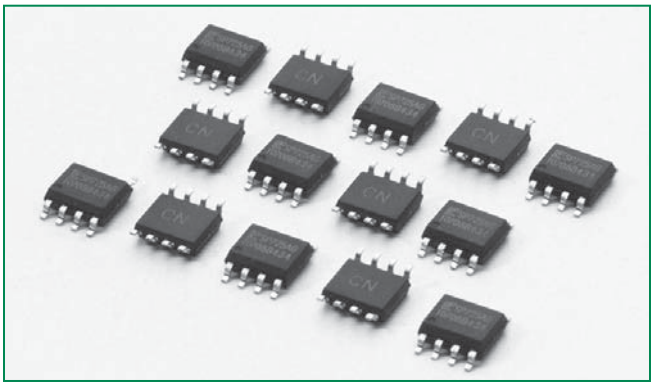
Part Number	Temp. Range (°C)	Package	Marking	Min. Order Qty.
SP724AHTG	-40 to 105	Tape and Reel	724G	3000

Embossed Carrier Tape & Reel Specification -- SOT23-6

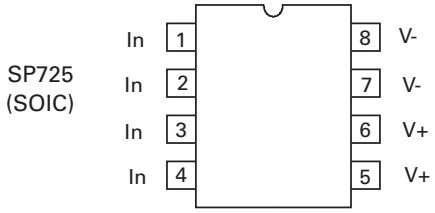
8mm TAPE AND REEL



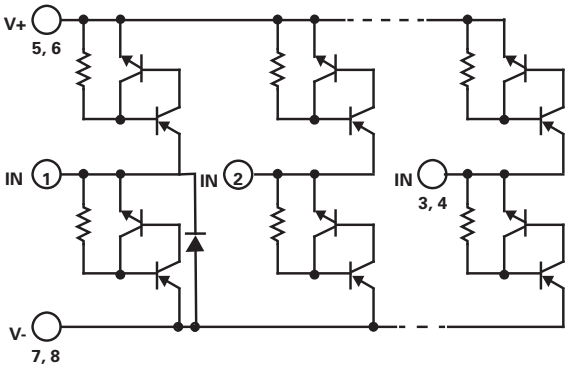
RoHS Pb GREEN SP725 Lead-Free/Green Series



Pinout



Functional Block Diagram



Description

The SP725 is an array of SCR/Diode bipolar structures for ESD and overvoltage protection of sensitive input circuits. The SP725 has 2 protection SCR/Diode device structures per input. There are a total of 4 available inputs that can be used to protect up to 4 external signal or bus lines. Overvoltage protection is from the IN (Pins 1 - 4) to V+ or V-.

The SCR structures are designed for fast triggering at a threshold of one $+V_{BE}$ diode threshold above V+ (Pin 5,6) or one $-V_{BE}$ diode threshold below V- (Pin 7,8). From an IN input, a clamp to V+ is activated if a transient pulse causes the input to be increased to a voltage level greater than one V_{BE} above V+. A similar clamp to V- is activated if a negative pulse, one V_{BE} less than V-, is applied to an IN input.

Refer to Fig 1 and Table 1 for further details. Refer to Application Note AN9304 and AN9612 for further detail.

Features

- ESD Interface per HBM Standards
  - IEC 61000-4-2, Direct Discharge ..... 8kV (Level 4)
  - IEC 61000-4-2, Air Discharge.....15kV (Level 4)
  - MIL-STD-3015.7 .....25kV
- Peak Current Capability
  - IEC 61000-4-5 8/20 µs Peak Pulse Current..... ± 14 A
  - Single Transient Pulse, 100 µs Pulse Width ..... ± 8 A
- Designed to Provide Over-Voltage Protection
  - Single-Ended Voltage Range to ..... +30V
  - Differential Voltage Range to ..... ±15V
- Fast Switching.....2ns Risetime
- Low Input Leakages.....5 nA at 25 °C Typical
- Low Input Capacitance.....5 pF Typical
- An Array of 4 SCR/Diode Pairs
- Operating Temperature Range.....-40 °C to 105 °C

Applications

- Microprocessor/Logic Input Protection
- Data Bus Protection
- Analog Device Input Protection
- Voltage Clamp

Absolute Maximum Ratings

Parameter	Rating	Units
Continuous Supply Voltage, (V+) - (V-)	+35	V
Forward Peak Current, I_{IN} to V_{CC} , I_{IN} to GND (Refer to Figure 6)	± 8 A, 100 µs	V
Peak Pulse Current, 8/20µs	± 14 A	V
ESD Ratings and Capability (Figure 1, Table 1) Load Dump and Reverse Battery (Note 2)		

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Thermal Information

Parameter	Rating	Units
Thermal Resistance (Typical, Note 1)	θ_{JA}	°C/W
SOIC Package	170	°C/W
Storage Temperature Range	-65 to 150	°C
Maximum Junction Temperature	150	°C
Maximum Lead Temperature (Soldering 10s) (SOIC - Lead Tips Only)	300	°C

Electrical Characteristics T_A = -40°C to 105°C, V_{IN} = 0.5V_{CC} , Unless Otherwise Specified

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Operating Voltage Range, V_{SUPPLY} = [(V+) - (V-)]	V_{SUPPLY}		-	2 to 30	-	V
Forward Voltage Drop IN to V-	V_{FWDL}	I_{IN} = 2A (Peak Pulse)	-	2	-	V
IN to V+	V_{FWDH}		-	2	-	V
Input Leakage Current	I_{IN}		-20	5	+20	nA
Quiescent Supply Current	$I_{QUIESCENT}$		-	50	200	nA
Equivalent SCR ON Threshold		(Note 3)	-	1.1	-	V
Equivalent SCR ON Resistance		V_{FWD}/I_{FWD} ; (Note 3)	-	0.5	-	Ω
Input Capacitance	C_{IN}			5	-	pF
Input Switching Speed	t_{ON}		-	2	-	ns

NOTES:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air
2. In automotive and battery operated systems, the power supply lines should be externally protected for load dump and reverse battery V+ and V- pins are connected to the same supply voltage source as the device or control line under protection, a current limiting resistor should be connected in series between the external supply and the SP725 supply pins to limit reverse battery current to within the rated maximum limits. Bypass capacitors of typically 0.01µF or larger from the V+ and V- pins to ground are recommended.
3. Refer to the Figure 3 graph for definitions of equivalent "SCR ON Threshold" and "SCR ON Resistance." These characteristics are given here for thumb-rule information to determine peak current and dissipation under EOS conditions.

ESD Capability

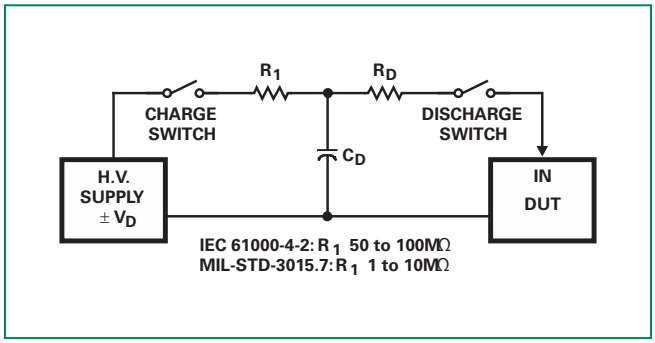
ESD capability is dependent on the application and defined test standard.The evaluation results for various test standards and methods based on Figure 1 are shown in Table 1.

The SP725 has a Level 4 HBM capability when tested as a device to the IEC 61000-4-2 standard. Level 4 specifies a required capability greater than 8kV for direct discharge and greater than 15kV for air discharge.

For the "Modified" MIL-STD-3015.7 condition that is defined as an "incircuit" method of ESD testing, the V+ and V- pins have a return path to ground and the SP725 ESD capability is typically greater than 25kV from 100pF through 1.5kΩ . By strict definition of MIL-STD-3015.7 using "pinto-pin" device testing, the ESD voltage capability is greater than 10kV.

For the SP725 EIAJ IC121 Machine Model (MM) standard, the ESD capability is typically greater than 2kV from 200pF with no series resistance.

Figure 1: Electrostatic Discharge Test



ESD Test Conditions - Table 1

STANDARD	TYPE/MODE	R_D	C_D	$\pm V_D$
IEC 61000-4-2 (Level 4)	HBM, Air Discharge	330 Ω	150pF	15kV
	HBM, Direct Discharge	330 Ω	150pF	8kV
MIL-STD-3015.7	Modified HBM	1.5k Ω	100pF	25kV
	Standard HBM	1.5k Ω	100pF	10kV
EIAJ IC121	Machine Model	0k Ω	200pF	2kV

Figure 2: Low Current SCR Forward Voltage Drop Curve

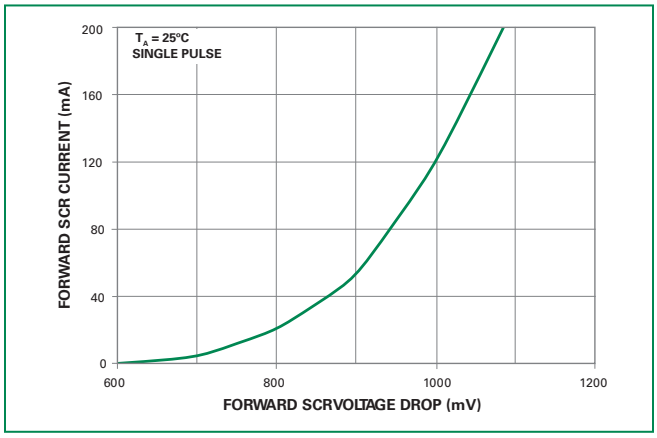
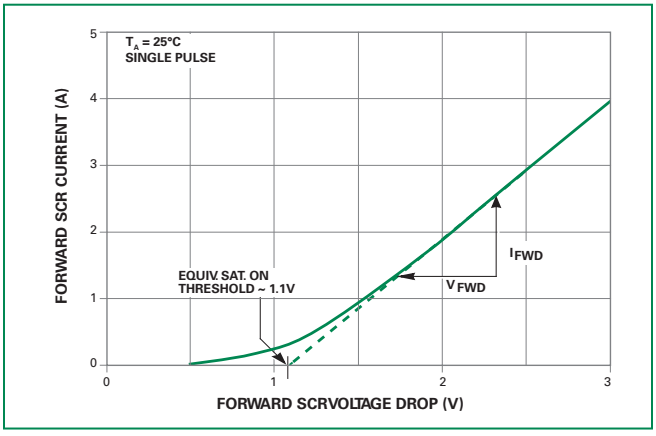


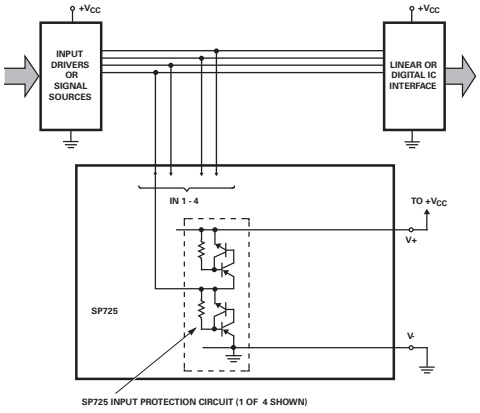
Figure 3: High Current SCR Forward Voltage Drop Curve



Lead-Free/Green SP725

Figure 4: Typical Application of the SP725

• (Application as an Input Clamp for Overvoltage, Greater than $1V_{BE}$ Above V+ or less than $-1V_{BE}$ below V-)



Peak Transient Current Capability for Long Duration Surges

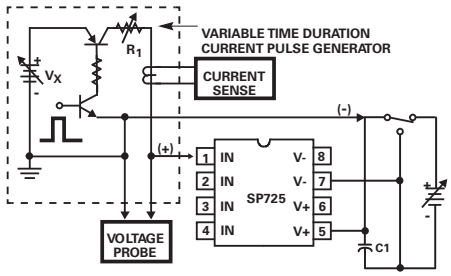
The peak transient current capability rises sharply as the width of the current pulse narrows. Destructive testing was done to fully evaluate the SP725 's ability to withstand a wide range of peak current pulses vs time. The circuit used to generate current pulses is shown in Figure 5.

The test circuit of Figure 5 is shown with a positive pulse input. For a negative pulse input, the (-) current pulse input goes to an SP725 'IN' input pin and the (+) current pulse input goes to the SP725 V- pin. The V+ to V- supply of the SP725 must be allowed to float. (i.e., It is not tied to the ground reference of the current pulse generator.) Figure 6 shows the point of overstress as defined by increased leakage in excess of the data sheet published limits.

The maximum peak input current capability is dependent on the ambient temperature, improving as the temperature is reduced. Peak current curves are shown for ambient temperatures of 25 ° C and 105 ° C and a 15V power supply condition. The safe operating range of the transient peak current should be limited to no more than 75% of the measured overstress level for any given pulse width as shown in the curves of Figure 6.

Note that adjacent input pins of the SP725 may be paralleled to improve current (and ESD) capability. The sustained peak current capability is increased to nearly twice that of a single pin.

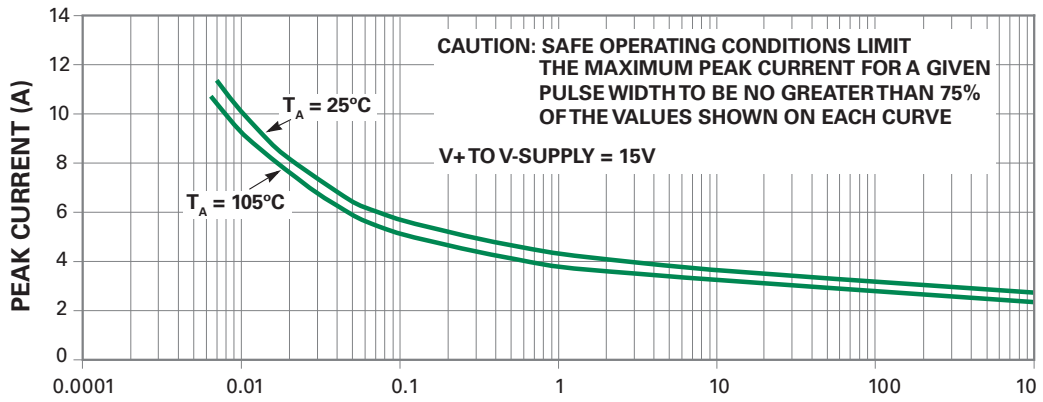
Figure 5: Typical SP725 Peak Current Test Circuit With a Variable Pulse Width Input



R_1 ~ 10Ω TYPICAL
V_X ADJ. 10V/A TYPICAL
C1 ~ 100µF

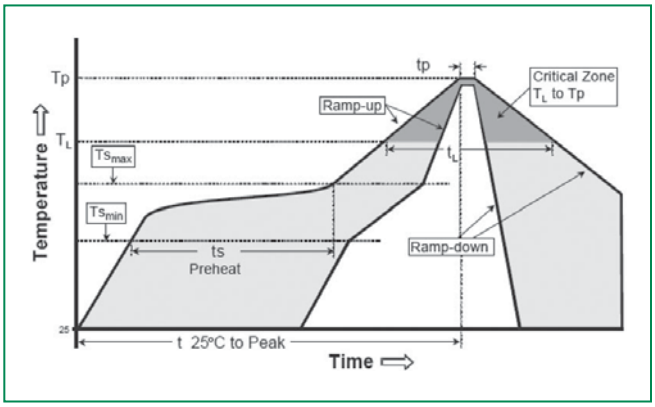
Figure 6: SP725 Typical Nonrepetitive Peak Current Pulse Capability

• Showing the Measured Point of Overstress in Amperes vs pulse width time in milliseconds

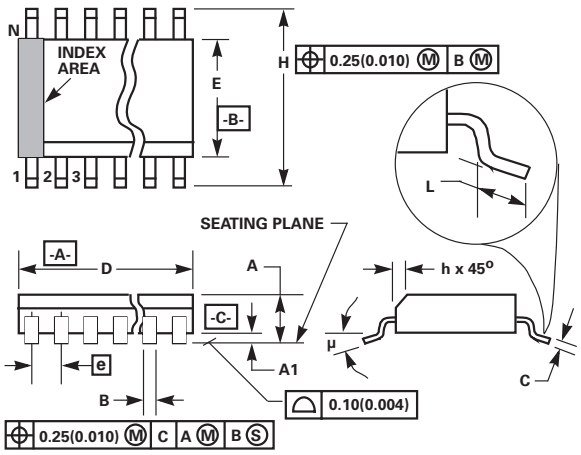


Soldering Parameters

Reflow Condition		Pb – Free assembly
Pre Heat	-Temperature Min ($T_{s(min)}$)	150°C
	-Temperature Max ($T_{s(max)}$)	200°C
	-Time (min to max) (t_s)	60 – 180 secs
Average ramp up rate (Liquidus) Temp (T_L) to peak		5°C/second max
$T_{S(max)}$ to T_L - Ramp-up Rate		5°C/second max
Reflow	-Temperature (T_L) (Liquidus)	217°C
	-Temperature (t_L)	60 – 150 seconds
Peak Temperature (T_P)		$250^{+0/-5}$ °C
Time within 5°C of actual peak Temperature (t_p)		20 – 40 seconds
Ramp-down Rate		5°C/second max
Time 25°C to peak Temperature (T_P)		8 minutes Max.
Do not exceed		260°C



Package Dimensions - Small Outline Plastic Packages (SOIC)

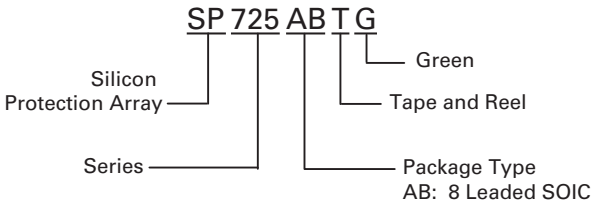


Package	SOIC				
Pins	8				
JEDEC	M8.15 MS-012-AA Issue C				
	Inches		Millimeters		Notes
	Min	Max	Min	Max	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.1890	0.1968	4.80	5.00	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	8		8		7
μ	0°	8°	0°	8°	-

Notes:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

Part Numbering System



Product Characteristics

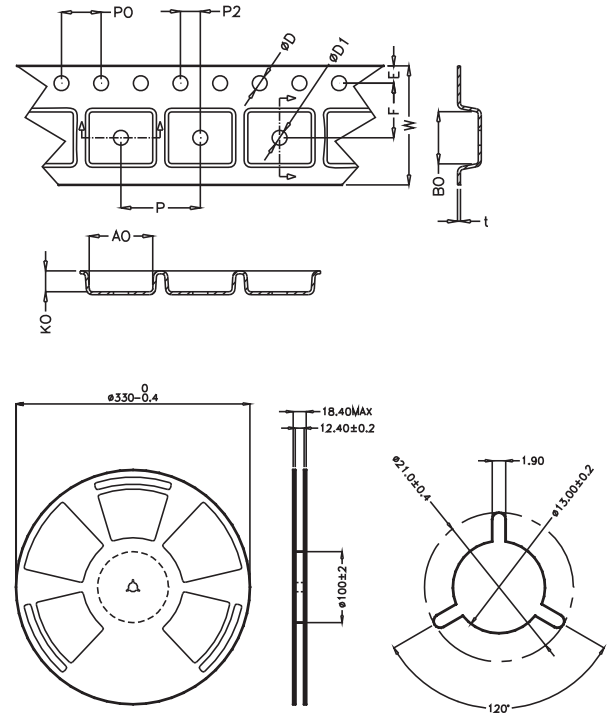
Lead Plating	Matte Tin
Lead Material	Copper Alloy
Lead Coplanarity	0.004 inches (0.102mm)
Subsitute Material	Silicon
Body Material	Molded Epoxy
Flammability	UL94-V-0

Notes:
1. All dimensions are in millimeters.
2. Dimensions include solder plating.
3. Dimensions are exclusive of mold flash & metal burr.
4. All specifications comply to JEDEC SPEC MO-203 ISSUE A.
5. Blo is facing up for mold and facing down for trim/form, i.e. reverse trim/form.
6. Package surface matte finish VDI 11-13.

Ordering Information

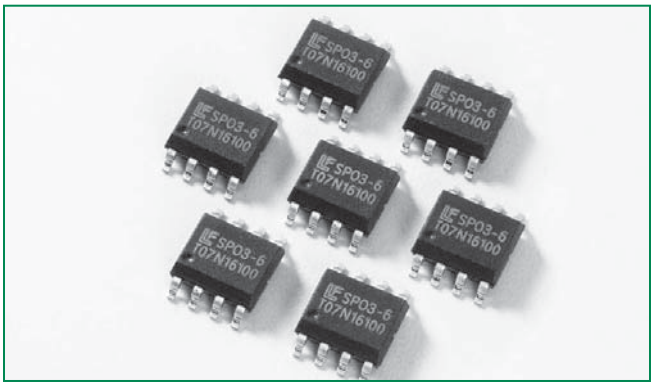
Part Number	Temp. Range (°C)	Package	Marking	Min. Order Qty.
SP725ABG	-40 to 105	8 Ld SOIC	SP725AG	1960
SP725ABTG	-40 to 105	8 Ld SOIC Tape and Reel	SP725AG	2500

Embossed Carrier Tape & Reel Specification - SOIC Package



Symbol	Millimetres		Inches	
	Min	Max	Min	Max
E	1.65	1.85	0.065	0.073
F	5.4	5.6	0.213	0.22
P2	1.95	2.05	0.077	0.081
D	1.5	1.6	0.059	0.063
D1	1.50 Min		0.059 Min	
P0	3.9	4.1	0.154	0.161
10P0	40.0 +/- 0.20		1.574 +/- 0.008	
W	11.9	12.1	0.468	0.476
P	7.9	8.1	0.311	0.319
A0	6.3	6.5	0.248	0.256
B0	5.1	5.3	0.2	0.209
K0	2	2.2	0.079	0.087
t	0.30 +/- 0.05		0.012 +/- 0.002	

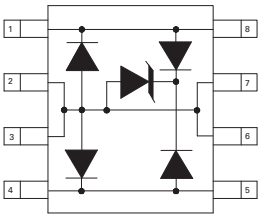
RoHS Pb GREEN SP03-6 (SO-8) Series



Agency Approvals - Pending

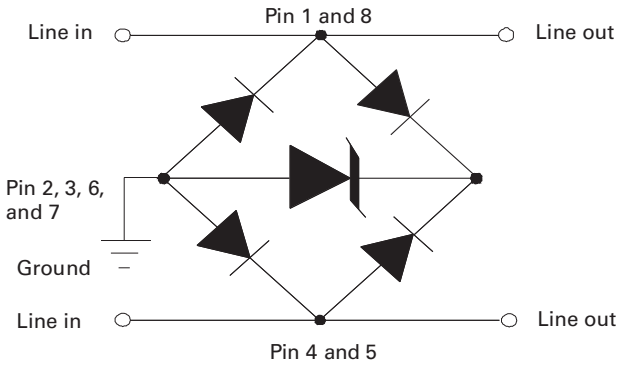
Agency	Agency File Number
UL	E128662

Pinout



SO-8 (Top View)

Functional Block Diagram



Description

This new broadband protection device from Littelfuse provides overvoltage protection for applications such as 10/100/1000 BaseT Ethernet, T3/E3 DS3 interfaces, ADSL2+, and VDSL2+. This new protector combines the TVS diode element with a diode rectifier bridge to provide both longitudinal and differential protection in one package. This design innovation results in a capacitive loading characteristic that is log-linear with respect to the signal voltage across the device. This reduces intermodulation (IM) distortion caused by a typical solid-state protection solution. The application schematic provides the connection information.

Features

- RoHS compliant
- MS-012 surface mount package (JEDEC SO-8)
- Low insertion loss, log-linear capacitance
- Combined longitudinal and metallic protection
- Clamping speed of nanoseconds
- UL 94V-0 epoxy molding
- Pending UL recognized component
- Low clamping voltage

Applications

- T1/E1 Line cards
- T3/E3 and DS3 Interfaces
- STS-1 Interfaces
- 10/100/1000 BaseT Ethernet

Absolute Maximum Ratings

Parameter	Rating	Units
Peak Pulse Current (8/20µs)	150	A
Peak Pulse Power (8/20µs)	2800	W
IEC 61000-4-2, Direct Discharge, (Level 4)	8	kV
IEC 61000-4-2, Air Discharge, (Level 4)	15	kV
IEC 61000-4-5 (8/20µs)	100	A
Bellcore GR 1089 (Intra-Building) (2/10µs)	100	A
ITU K.20 (5/310µs)	40	A

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Thermal Information

Parameter	Rating	Units
SOIC Package	170	°C/W
Storage Temperature Range	-65 to 150	°C
Maximum Junction Temperature	150	°C
Maximum Lead Temperature (Soldering 10s) (SOIC - Lead Tips Only)	300	°C

Electrical Characteristics (T_{OP} = 25°C)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Reverse Stand-Off Voltage	V_{RWM}	-	-	-	6	V
Reverse Breakdown Voltage	V_{BR}	I_T= 1mA	6.8	-	-	V
Reverse Leakage Current	I_R	V_{RWM}= 6V, T= 25°C	-	-	25	µA
Clamping Voltage, Line-Ground	V_C	I_{PP}= 50A, t_p=8/20 µs	-	-	15	V
Clamping Voltage, Line-Ground	V_C	I_{PP}= 100A, t_p=8/20 µs	-	-	20	V
Junction Capacitance	C_j	V_R=0V, f= 1MHz	-	16	25	pF
		V_R=0V, f= 1MHz	-	8	12	pF

Figure 1: Non-repetitive Peak Pulse Current vs. Pulse Time

Figure 2: Current Derating Curve

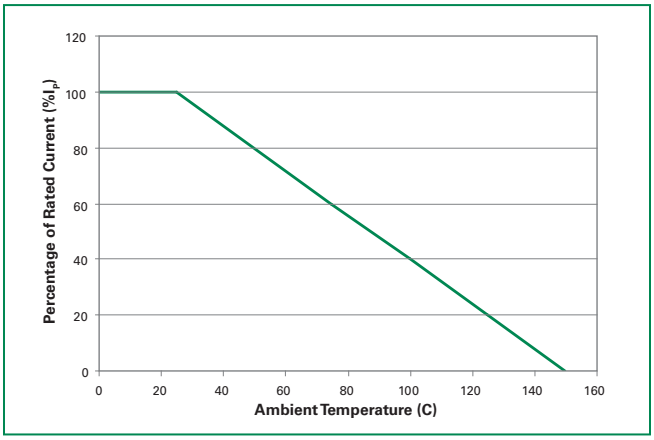


Figure 3: Pulse Waveform

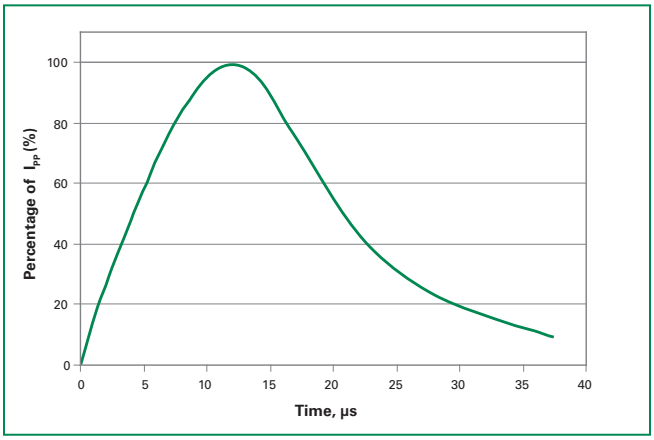


Figure 4: Clamping Voltage vs. Peak Pulse Current

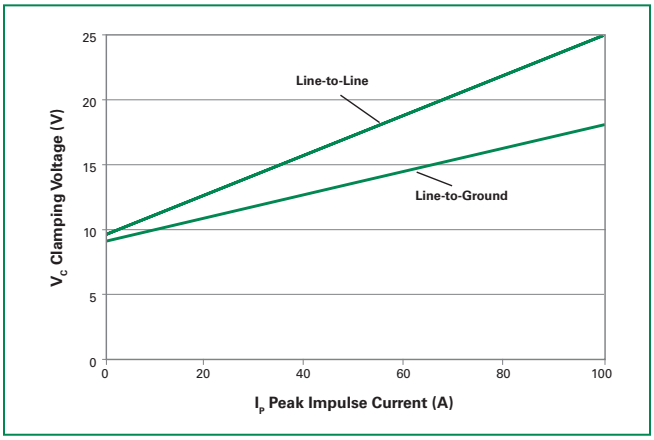


Figure 5: Capacitance vs. Reverse Voltage

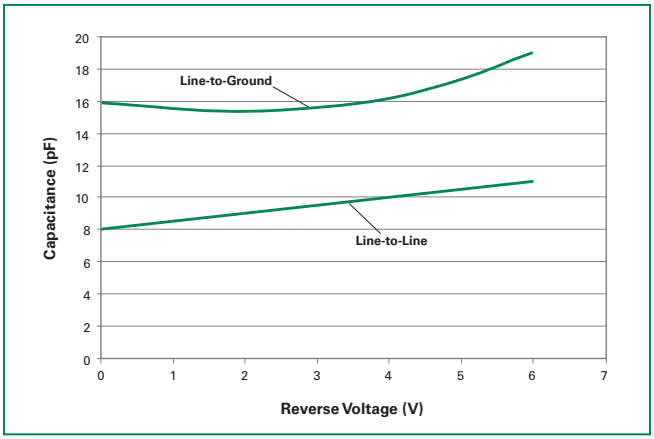
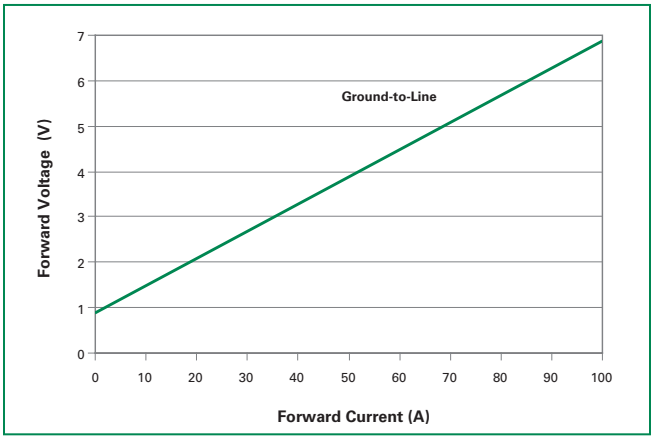
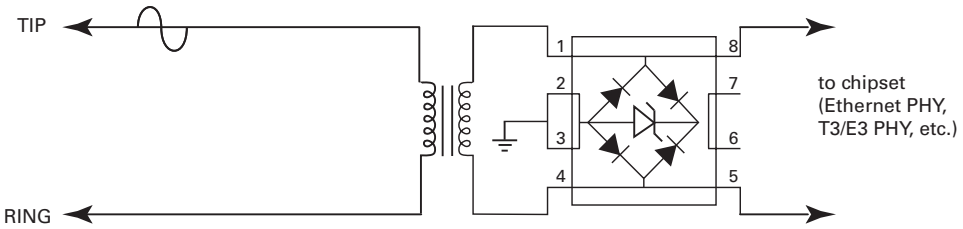


Figure 6: Forward Voltage vs. Forward Current



Application Example

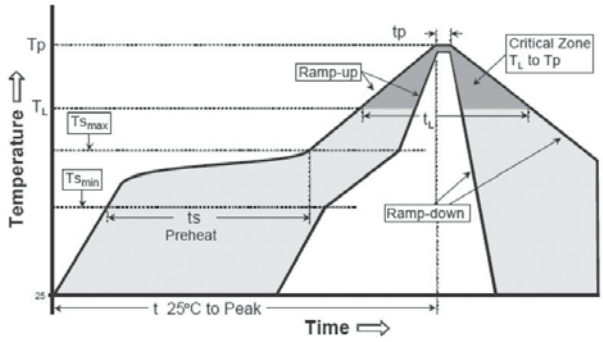
The following schematic shows a high-speed data interface protection solution. The SP03-6 provides both metallic (differential) and longitudinal (common mode) protection from lightning induced surge events. Its surge rating is compatible with the intra-building surge requirements of Telcordia's GR-1089-CORE, and the Basic Level Recommendations of ITU K.20 and .21. This device protects against both positive and negative induced surge events. The TeleLink fuse provides overcurrent protection for the long term 50/60 Hz power fault events.



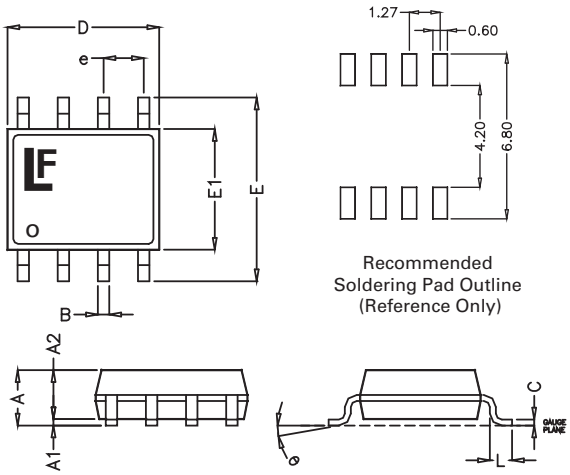
TeleLink (0461 1.25) SP03-6

Soldering Parameters

Reflow Condition		Pb – Free assembly
Pre Heat	-Temperature Min ($T_{s(min)}$)	150°C
	-Temperature Max ($T_{s(max)}$)	200°C
	-Time (min to max) (t_s)	60 – 180 secs
Average ramp up rate (Liquidus) Temp (T_L) to peak		3°C/second max
$T_{S(max)}$ to T_L - Ramp-up Rate		3°C/second max
Reflow	-Temperature (T_L) (Liquidus)	217°C
	-Temperature (t_L)	60 – 150 seconds
Peak Temperature (T_P)		$250^{+0/-5}$ °C
Time within 5°C of actual peak Temperature (t_p)		20 – 40 seconds
Ramp-down Rate		6°C/second max
Time 25°C to peak Temperature (T_P)		8 minutes Max.
Do not exceed		260°C

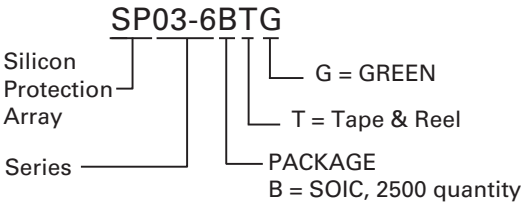


Package Dimensions - Mechanical Drawings and Recommended Solder Pad Outline



Package	MS-012 (SO-8)			
Pins	8			
JEDEC	MO-223 Issue A			
	Millimetres		Inches	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
A2	1.25	1.65	0.043	0.065
B	0.31	0.51	0.012	0.020
c	0.017	0.25	0.007	0.010
D	4.80	5.00	0.189	0.197
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
L	0.40	1.27	0.016	0.050

Part Numbering System



Product Characteristics

Lead Plating	Matte Tin
Lead Material	Copper Alloy
Lead Coplanarity	0.004 inches (0.102mm)
Subsitute Material	Silicon
Body Material	Molded Epoxy
Flammability	UL94-V-0

Notes :
1. All dimensions are in millimeters
2. Dimensions include solder plating.
3. Dimensions are exclusive of mold flash & metal burr.
4. All specifications comply to JEDEC SPEC MO-223 Issue A
5. Blo is facing up for mold and facing down for trim/form, i.e. reverse trim/form.
6. Package surface matte finish VDI 11-13.

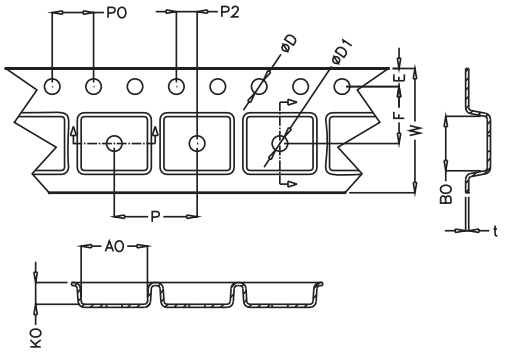
Part Marking System

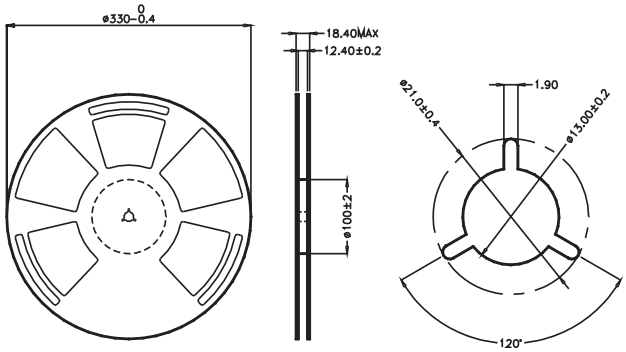
First Line: Part number
Second Line: Date code

Ordering Information

Part Number	Package	Marking	Min. Order Qty.
SP03-6BTG	SOIC Tape & Reel	SP03-6	2500

Embossed Carrier Tape & Reel Specification - SOIC Package

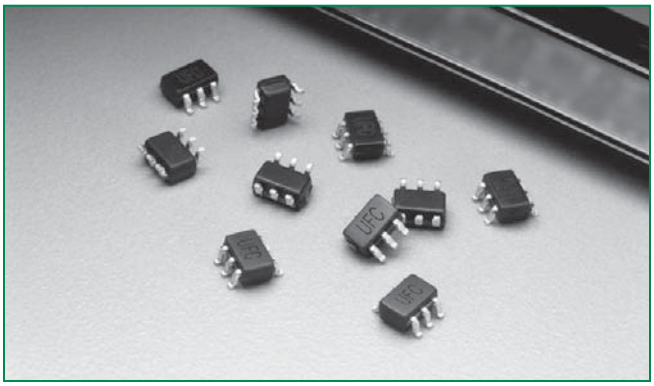




Dimensions

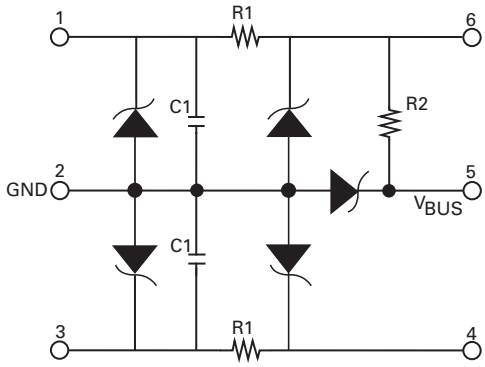
	Millimetres		Inches	
	Min	Max	Min	Max
E	1.65	1.85	0.065	0.073
F	5.4	5.6	0.213	0.22
P2	1.95	2.05	0.077	0.081
D	1.5	1.6	0.059	0.063
D1	1.50 Min		0.059 Min	
P0	3.9	4.1	0.154	0.161
10P0	40.0 +/- 0.20		1.574 +/- 0.008	
W	11.9	12.1	0.468	0.476
P	7.9	8.1	0.311	0.319
A0	6.3	6.5	0.248	0.256
B0	5.1	5.3	0.2	0.209
K0	2	2.2	0.079	0.087
t	0.30 +/- 0.05		0.012 +/- 0.002	

SPUSB1 Series



Functional Block Diagram

SC70-6



Description

The Littelfuse SPUSB1 Series is a multifunctional USB port protection network designed to provide ESD protection, EMI/RFI filtering and line termination for a single USB 1.1 port. The SPUSB1 can replace a minimum of ten typically larger "discrete" devices resulting in inventory and placement cost savings.

The SPUSB1 Series combines Transient Voltage Suppression (TVS) avalanche diodes, EMI/RFI filtering components (R1 and C1), and a1.5kΩ termination resistor (R2). The filtering components are included to satisfy recommendations in the USB 1.1 specification, and the 1.5kΩ resistor (R2) is included as a pull-up resistor to VBUS.

The SPUSB1 Series can be used for termination and protection of"upstream" USB devices such as PDAs, digital cameras, scanners and hubs which are often at risk from transient voltage surges and electromagnetic interference from both internal and external sources.

To support a wide range of circuit conditions, Littelfuse offers three resistance values for the series resistor (R1). The series resistance plus the USB driver output resistance must be close to the USB cable's characteristic impedance of 45Ω (90Ω balanced) to minimize transmission line reflections.

Features

- One upstream USB port terminator, EMI filter and transient overvoltage protector in a single surface-mount package
- Compact SC70 package saves board space and lowers manufacturing costs compared to discrete solutions
- ESD protection to 30kV contact discharge per MIL-STD- 883D, method 3015
- ESD protection to 15kV contact discharge per IEC 61000-4-2 international standard

Applications

- Desktop/Laptop PCs
- USB peripherals (printers, scanners, zip drives)
- PDAs / wireless handsets
- Digital cameras
- MP3 Players
- Cable Modems

Absolute Maximum Ratings

Parameter	Rating	Units
Supply Voltage V_{BUS}	5.5	V
DC Power per Resistor	100	mW
Package Power	200	mW
Temperature Range:		
Operating	-40 to +85	°C
Storage	-65 to +150	

Electrical Characteristics Standard at 25°C unless specified otherwise

Parameter		Min	Typ	Max	Unit
Resistance R1 (SPUSB1AJT only)		6	12	14	Ω
Resistance R1 (SPUSB1CJT only)		26	33	40	Ω
Resistance R1 (SPUSB1BJT only)		18	22	26	Ω
Resistance R2		1.2	1.5	1.8	kΩ
Capacitance C1 @ 2.5 v DC, 1MHz		38	47	56	pF
Diode Leakage at 3.3v			1	100	nA
Diode Reverse Blas Stand-off Voltage, 1= 10µA		5.5			V
Signal Clamp Voltage:					
Positive Clamp, 10mA		5.6	6.8	8.0	V
Negative Clamp, 10mA		-1.2	-0.8	-0.4	V
In-system ESD Withstand Voltage[1]					
Human Body Model (MIL-STD-883D, method 3015)		±30			kV
IEC 61000-4-2, contact discharge method (I/O pins)		±15			kV
IEC 61000-4-2, contact discharge method (V_{BUS} pin)		±25			kV
Clamping Voltage During ESD Discharge [1]	Positive		10		V
MIL-STD-883D (Method 3015), 8kV	Negative		-5		V

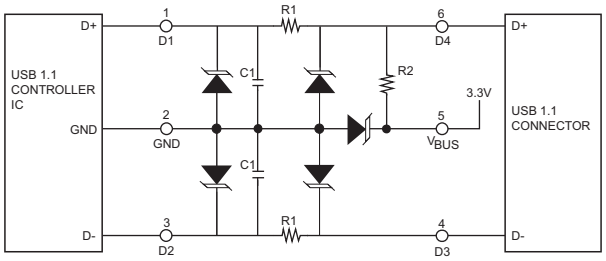
Note:

1. ESD applied to input/outputVDD pins with respect to GND, one at a time.
   Clamping Voltage is measured at the opposite side of the EMI filter to the ESD pin (ie: if ESD is applied to pin1 then clamping voltage is measured at pin 6). Unused pins are open.
   These parameters guaranteed by design.

Typical Application of the SPUSB1

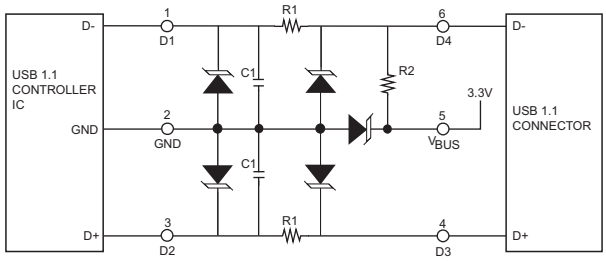
Full-Speed Devices (12Mbits per second)

For full speed operation the pull-up resistor R2 is connected to the D+ pin.



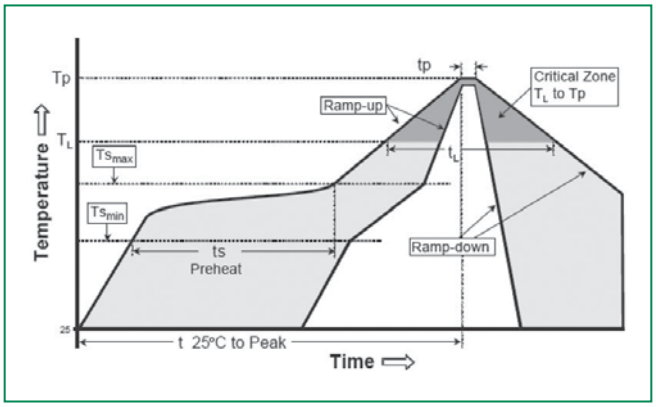
Low-Speed Devices (1.5Mbits per second)

Low speed connection requires the pull-up resistor R2 to be connected to the Dpin. Please note the reversal of the D- and D+ pins on Figure 2 versus Figure 1.



Soldering Parameters

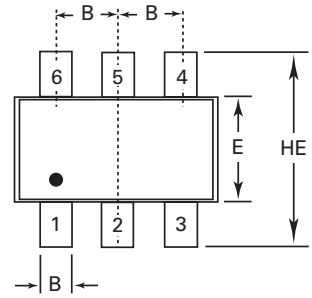
Reflow Condition		Pb – Free assembly
Pre Heat	-Temperature Min ($T_{s(min)}$)	150°C
	-Temperature Max ($T_{s(max)}$)	200°C
	-Time (min to max) (t_s)	60 – 180 secs
Average ramp up rate (Liquidus) Temp (T_L) to peak		5°C/second max
$T_{S(max)}$ to T_L - Ramp-up Rate		5°C/second max
Reflow	-Temperature (T_L) (Liquidus)	217°C
	-Temperature (t_L)	60 – 150 seconds
Peak Temperature (T_P)		$250^{+0/-5}$ °C
Time within 5°C of actual peak Temperature (t_p)		20 – 40 seconds
Ramp-down Rate		5°C/second max
Time 25°C to peak Temperature (T_P)		8 minutes Max.
Do not exceed		260°C



Product Characteristics

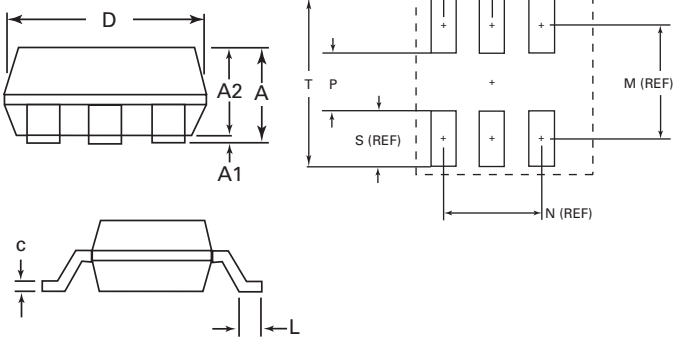
Lead Plating	Tin-Lead
Lead Material	Copper Alloy
Lead Coplanarity	0.004 inches (0.102mm)
Subsitute Material	Silicon
Body Material	Molded Epoxy
Flammability	UL94-V-0

Package Dimensions - SC70



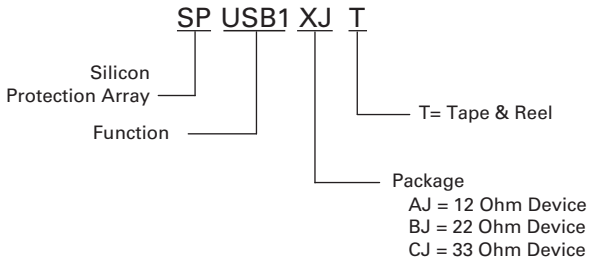
SPUSB1AJT - SC70-6
SPUSB1BJT - SC70-6
SPUSB1CJT - SC70-6

Recommended Pad Layout



Package	SC70-6			
Pins	6			
JEDEC	MO-203 Issue A, M8.15 MS-012-AA Issue C			
	Millimeters		Inches	
	Min	Max	Min	Max
A	0.80	1.10	0.031	0.043
A1	0.00	0.10	0.000	0.004
A2	0.70	1.00	0.028	0.039
B	0.15	0.30	0.006	0.012
c	0.08	0.25	0.003	0.010
D	1.85	2.25	0.073	0.089
E	1.15	1.35	0.045	0.053
e	0.65 BSC		0.026 BSC	
HE	2.00	2.40	0.079	0.094
L	0.26	0.46	0.010	0.018
M	-	1.60	-	0.063
N	-	1.30	-	0.052
O	-	0.65	-	0.026
P	-	0.70	-	0.058
R	-	0.35	-	0.014
S	-	0.90	-	0.035
T	-	2.50	-	0.098

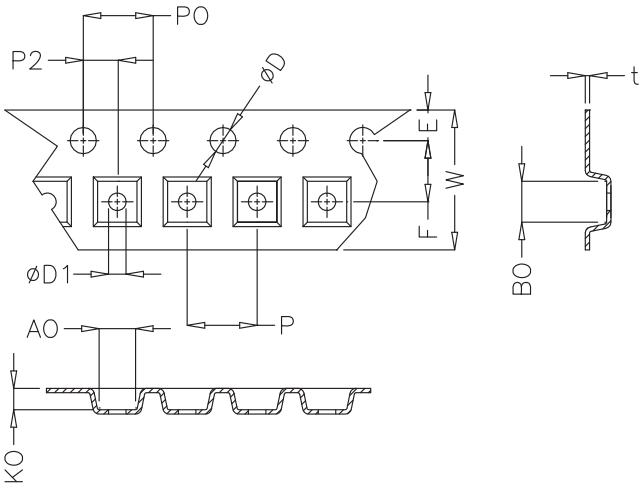
Part Numbering System



Ordering Information

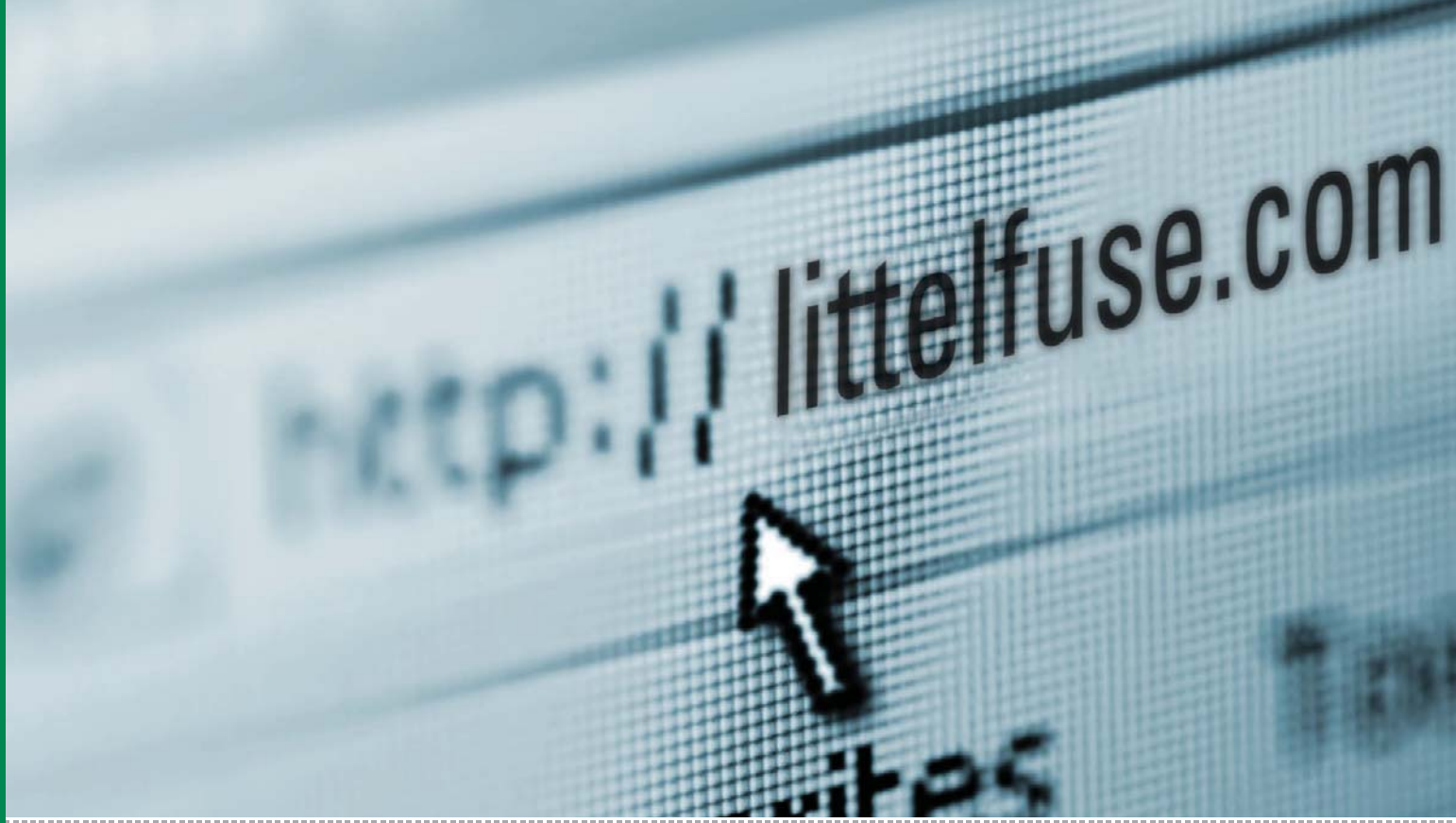
Part Number	R1 (Ohm)	R2 (KOhm)	C1 (pF)	Device Brand	PKG Type	#/Reel
SPUSB1AJT	12	1.5	47	UFA	SC70-6	3000
SPUSB1BJT	22	1.5	47	UFB	SC70-6	3000
SPUSB1CJT	33	1.5	47	UFC	SC70-6	3000

Embossed Carrier Tape & Reel Specification - SC70-6



Dimensions

Symbol	Millimetres		Inches	
	Min	Max	Min	Max
E	1.65	1.85	0.065	0.073
F	3.45	3.55	0.135	0.139
P2	1.95	2.05	0.077	0.081
D	1.40	1.60	0.055	0.063
D1	1.00	1.25	0.039	0.049
P0	3.90	4.10	0.154	0.161
10P0	40.0 +/- 0.20		1.574 +/- 0.008	
W	7.70	8.10	0.303	0.318
P	3.90	4.10	0.153	0.161
A0	2.14	2.34	0.084	0.092
B0	2.24	2.44	0.088	0.096
K0	1.12	1.32	0.044	0.051
t	0.27 max		0.010 max	



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Printed Product Catalogs—For offline and off-the-shelf convenience, our printed product catalogs include data sheets, selection tables and tutorials covering all of our core technologies. Contact your Littelfuse product representative or visit **www.littelfuse.com/catalogs** to check availability.

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www.littelfuse.com/catalogs

Littelfuse offers several technologies to protect sensitive electronic circuits from excess current resulting from overloads, short circuits, power cross or ground faults. Our overcurrent protection product line includes:

Fuses Littelfuse offers the world's broadest range of fuse types and ratings, including cartridge, leaded, surface mount and thin film designs

PTC Protectors Positive Temperature Coefficient thermistor technology provides resettable current-limiting protection

Littelfuse offers multiple technologies for overvoltage suppression and switching to protect sensitive electronic circuits from excessive voltage resulting from electrostatic discharge (ESD), load switching or lightning strikes. Our overvoltage protection product line includes:

Varistors Littelfuse offers surface mount Multi-Layer Varistors (MLVs) and industrial Metal Oxide Varistors (MOVs) to protect against transients

GDTs Gas Discharge Tubes (GDTs) to dissipate voltage through a contained plasma gas

Thyristors Littelfuse's solid state switches control the flow of current in a wide range of appliances, tools and equipment

SIDACtor® Devices Overvoltage protection specifically designed for telecom and datacom requirements

TVS Diodes Silicon transient voltage suppression (TVS) devices

SPAs Silicon Protection Arrays designed for analog and digital signal line protection

PulseGuard® ESD Suppressors Small, fast-acting Electrostatic Discharge (ESD) suppressors

FORM NO. EC113
Revision Code: EC2113v1E0807